SEGA™ SERVICE MANUAL

GENESIS
MEGA DRIVE PAL
MEGA CD/SEGA CD

NO.	010
ISSUED	APRIL, 1994

CONTENTS

This manual contains IC specification to be added to the manuals issued previously.

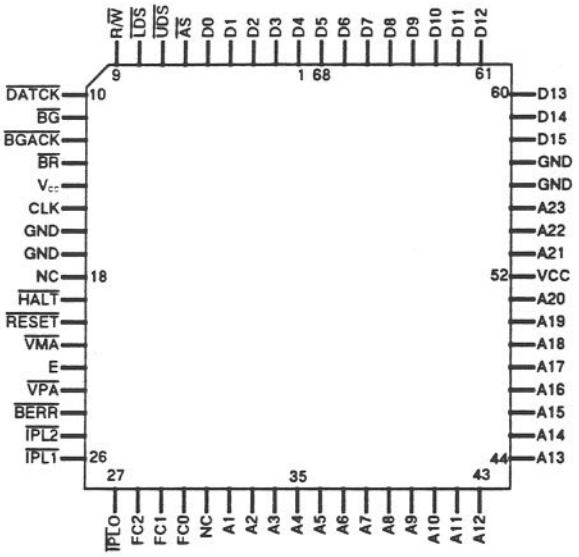
Sega Enterprises, Ltd.

PARTS SPECIFICATIONS

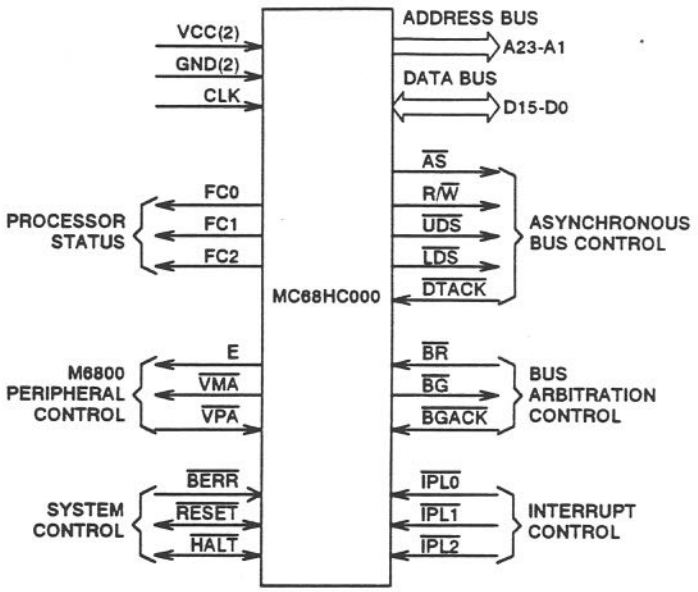
IC1 16/32-bit Microprocessor

IC MC68HC000FN8 IC HD68HC000CP8

■ Top View & Pin Layout



■ Signal Description



■ Description

No.	Pin Name	I/O	Function
1	D_4	I/O	Data bus
2	D_3		
3	D_2		
4	D_1		
5	D_0		
6	$\overline{AS}$	O	Address strobe
7	$\overline{UDS}$	O	Upper data strobe
8	$\overline{LDS}$	O	Lower data strobe
9	R/$\overline{W}$	O	Read/Write
10	$\overline{DTACK}$	I	Data transfer Acknowledge
11	$\overline{BG}$	O	Bus grant
12	$\overline{BGACK}$	I	Bus grant acknowledge
13	$\overline{BR}$	I	Bus request
14	V_{CC}	–	Power supply
15	CLK	I	Clock
16	V_{SS}	–	GND
17	V_{SS}		
18	NC	–	Not connected
19	$\overline{HALT}$	I/O	Halt
20	$\overline{RES}$	I/O	Reset
21	$\overline{VMA}$	O	Vaild memory address
22	E	O	Enable

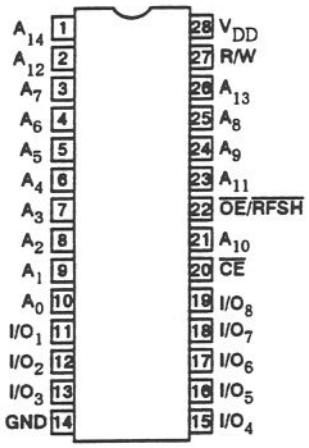
No.	Pin Name	I/O	Function
23	$\overline{VPA}$	I	Vaild peripheral address
24	$\overline{BERR}$	I	Bus error
25	$\overline{IPL_2}$	I	Interrupt control
26	$\overline{IPL_1}$		
27	$\overline{IPL_0}$		
28	FC_2	O	Processor status
29	FC_1		
30	FC_0		
31	NC	–	
32	A_1	O	Address bus
33	A_2		
34	A_3		
35	A_4		
36	A_5		
37	A_6		
38	A_7		
39	A_8		
40	A_9		
41	A_{10}		
42	A_{11}		
43	A_{12}		
44	A_{13}		
45	A_{14}		

No.	Pin Name	I/O	Function
46	A_{15}	O	Address bus
47	A_{16}		
48	A_{17}		
49	A_{18}		
50	A_{19}		
51	A_{20}		
52	V_{CC}	–	Power supply
53	A_{21}	O	Address bus
54	A_{22}		
55	A_{23}		
56	V_{SS}	–	GND
57	V_{SS}		
58	D_{15}	I/O	Data bus
59	D_{14}		
60	D_{13}		
61	D_{12}		
62	D_{11}		
63	D_{10}		
64	D_9		
65	D_8		
66	D_7		
67	D_6		
68	D_5		

IC2/3 32768 Word × 8bit CMOS Pseudo-Static RAM

IC HM65256BLFP-10 IC TC51832FL-10

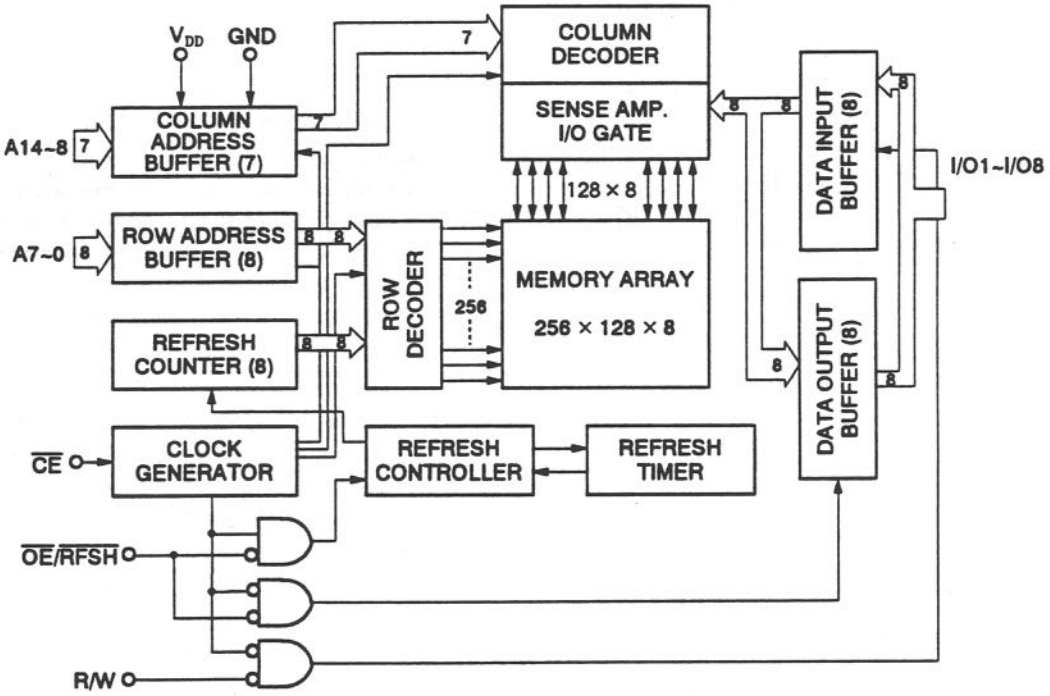
■ Top View & Pin Layout



■ Pin name

Pin Name	Function
A0~A14	Address input
R/W	Read/write input
$\overline{OE}/\overline{RESH}$	Output enable input/refresh input
$\overline{CE}$	Chip enable input
I/O1~I/O8	Data input/output
V_{DD}	Power supply
GND	Ground

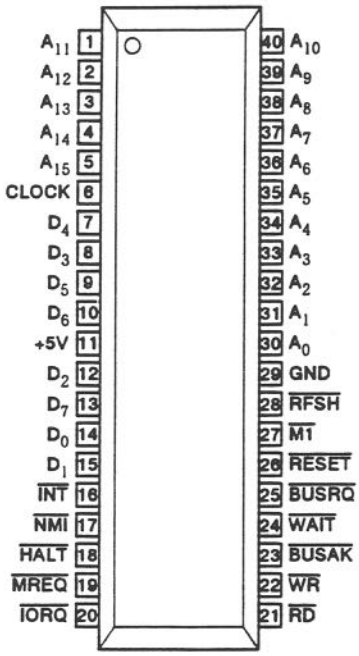
■ Block Diagram



IC4 Z80A Central Processing Unit

IC Z80A
315-0041

■ Top View & Pin Layout



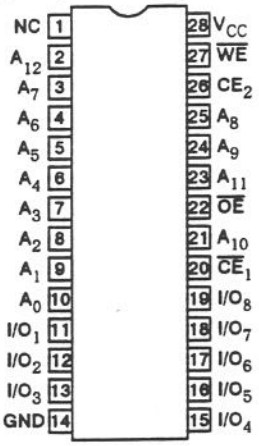
■ Description

Pin	Pin Name	I/O	Function
30~40 1~5	A0~A15	3-STATE O	System address bus.
15~12 7~10	D0-D7	3-STATE I/O	System data bus.
6	$\overline{\text{CLOCK}}$	I	Receives a +5V single-phase clock signal.
16	$\overline{\text{INT}}$	I	Active "Low". If the input/output device issues a signal that requests an interrupt to the Z80 CPU and the interrupt enable flag is zero, this interrupt request is accepted at the end of the instruction that is currently in progress.
17	$\overline{\text{NMI}}$	I	Active "Low". This is an interrupt request that has priority over $\overline{\text{INT}}$ and cannot be inhibited by the software. $\overline{\text{NMI}}$ is always accepted, and when the instruction that is currently in progress finishes, interrupt processing is started and the Z80 CPU automatically starts from address 0066H.
18	$\overline{\text{HALT}}$	O	Active "Low". This indicates that the HALT instruction is being executed. Executes the NOP instruction internally and also refreshes memory. The halt state is released by $\overline{\text{RESET}}$. $\overline{\text{NMI}}$ or $\overline{\text{INT}}$ (when enabled).
19	$\overline{\text{MREQ}}$	3-STATE O	Active "Low". This indicates that the address bus outputs the effective memory address for memory read/write.
20	$\overline{\text{IORQ}}$	3-STATE O	Active "Low". This indicates that the low-order 8 bits of the address bus output effective addresses of the input/output device for the read/write operation with this device. This is output together with $\overline{\text{MI}}$ during an interrupt response to indicate the response.
21	$\overline{\text{RD}}$	3-STATE O	Active "Low". This indicates the timing with which data from the memory or input/output device is read.
22	$\overline{\text{WR}}$	3-STATE O	Active "Low". This indicates that the effective data to be written to the memory or input/output device the address of which is specified is on the data bus.
23	$\overline{\text{BUSAK}}$	O	When the bus request is acknowledged, this informs the bus master which outputs the bus request that the system bus can be controlled.
24	$\overline{\text{WAIT}}$	I	Active "Low". Signal to inform the CPU that the memory or input/output device the address of which is specified is not ready to send data. The CPU is waiting when this signal is input.
25	$\overline{\text{BUSRQ}}$	I	Active "Low". This has priority over $\overline{\text{NMI}}$ and is accepted at the end of the machine cycle that is currently in progress. This is set to "Low" when a bus master other than the CPU wants to control the system bus.
26	$\overline{\text{RESET}}$	I	Active "Low". This resets the interrupt enable flag, interrupt vector register and memory refresh register of the program counter to set the interrupt mode to mode 0, thus initializing the Z80 CPU.
27	$\overline{\text{MI}}$	O	Active "Low". This indicates that the machine cycle being executed is an OP code fetch cycle.
28	$\overline{\text{RFSH}}$	O	Active "Low". This indicates that the address for refreshing the dynamic RAM is output to the low-order 7 bits of the address bus. $\overline{\text{MREQ}}$ also goes "Low" at this time.

IC5 65536 bit Static CMOS RAM

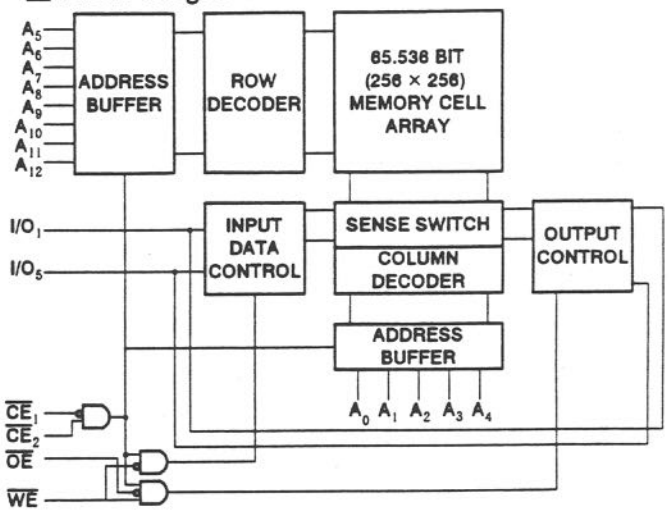
IC UPD4364G-15L IC MB8464A-80 IC MB8464A-10LL

■ Top view & Pin Layout



A_0~A_{12} : ADDRESS INPUT
OE : OUTPUT ENABLE INPUT
I/O_1~I/O_8 : DATA IN/OUTPUT
V_{CC} : +5V POWER SUPPLY
$\overline{CE}_1$, CE_2 : CHIP ENABLE 1, 2 INPUT
GND : GROUND
$\overline{WE}$: WRITE ENABLE INPUT
NC : NO CONNECTION

■ Block Diagram



■ Operation Mode

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	MODE	OUTPUT STATE	POWER SUPPLY CURRENT
H	×	×	×	Non-select (Power down)	High impedance	I_{SB}
×	L	×	×			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

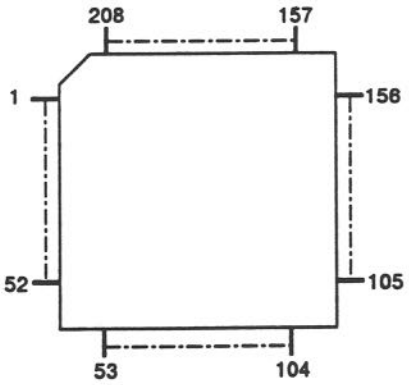
IC6 CUSTOM IC

IC CUSTOM CHIP SGE FC1004
315-5487-R

IC CUSTOM CHIP SGE FC1004
837-5487-01R

IC CUSTOM CHIP SGE FC1004
315-5487-01R

■ Top View & Pin Layout



■ Description

Pin No.	Name	I/O	Function
1	SD0	I	Dual port RAM interface signals.
2	SD1		
3	SD2		
4	SD3		

Pin No.	Name	I/O	Function
5	SD4	I	Dual port RAM interface signals.
6	SD5		
7	SD6		
8	SD7		

Pin No.	Name	I/O	Function
9	$\overline{SE1}$	O	Dual port RAM interface signals.
10	$\overline{SE0}$		
11	$\overline{SC}$		
12	$\overline{RAS1}$		
13	$\overline{CAS1}$		
14	$\overline{WE1}$		
15	$\overline{WE0}$		
16	$\overline{OE1}$		
17	RD0	I/O	Dual port RAM interface signals.
18	RD1		
19	RD2		
20	RD3		
21	VSS	–	GND
22	RD4	I/O	Dual port RAM interface signals.
23	RD5		
24	RD6		
25	RD7		
26	AD0		
27	AD1		
28	AD2		
29	AD3		
30	AD4		
31	AD5		
32	AD6		
33	AD7		
34	VIDEO AVSS	–	VIDEO+PSG
35	R (ANALOG)	O	
36	G (ANALOG)		
37	B (ANALOG)		
38	VIDEO AVDD	–	
39	$\overline{YS}$	O	
40	SPA/B	I/O	
41	$\overline{VSYNC}$	O	
42	$\overline{CSYNC}$	I/O	VIDEO+PSG
43	$\overline{HSYNC}$	I/O	
44	VDD	–	Power supply.
45	$\overline{M3}$	I	
46	$\overline{NTSC}$		
47	$\overline{VPA}$	O	68000 interface signals.
48	$\overline{HALT}$		
49	$\overline{RESET}$		
50	FC0	I	
51	FC1		
52	$\overline{MREQ}$	I/O	Z80 interface signals.
53	VSS	–	GND
54	AUSS	–	FM
55	MOR	O	
56	MOL	–	
57	SOUND	–	
58	$\overline{SOUND}$	I/O	Use this pin set to open certainly.

Pin No.	Name	I/O	Function
59	$\overline{ZRES}$	I/O	Z80 interface signals.
60	$\overline{ZBAK}$	I	Z80 interface signals.
61	$\overline{NMI}$	O	
62	$\overline{ZBR}$	I/O	
63	$\overline{WAIT}$		
64	$\overline{EOE}$	O	P-SRAM interface.
65	$\overline{NOE}$		
66	$\overline{ZRAM}$	O	SRAM interface.
67	$\overline{REF}$		
68	$\overline{CAS2}$	O	
69	$\overline{RAS2}$		
70	$\overline{ASEL}$		
71	$\overline{ROM}$		
72	$\overline{FDC}$		
73	$\overline{FDWR}$		
74	$\overline{CEO}$		
75	$\overline{TIME}$		
76	$\overline{CART}$	I	
77	IA14	O	
78	$\overline{WRES}$	I	
79	$\overline{DISK}$	I/O	
80	VDD	–	Power supply.
81	TEST0	I/O	Test signal. (Set to "0" certainly.)
82	TEST1	I	Test signals. (These pins set to all open.)
83	TEST2		
84	TEST3		
85	PC0	I/O	Joy pad interface.
86	PC1		
87	PC2		
88	PC3		
89	PC4		
90	PC5		
91	PC6		
92	VSS	–	GND
93	PB0	I/O	Joy pad Interface.
94	PB1		
95	PB2		
96	PB3		
97	PB4		
98	PB5		
99	PB6		
100	PA0		
101	PA1		
102	PA2		
103	PA3		
104	PA4		
105	PA5		
106	PA6		
107	$\overline{JAP}$	I/O	
108	$\overline{FRES}$		

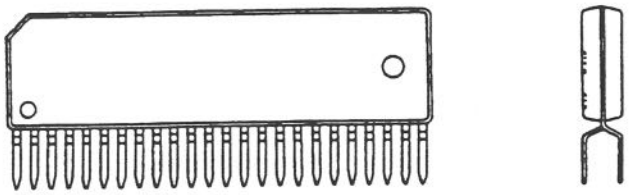
Pin No.	Name	I/O	Function
109	ZV	I/O	Use this pin set to open certainly.
110	VZ		
111	IO		
112	ZA0	I/O	Z80 address bus.
113	ZA1		
114	ZA2		
115	ZA3		
116	ZA4		
117	ZA5		
118	ZA6		
119	ZA7		
120	ZA8		
121	ZA9		
122	ZA10		
123	ZA11		
124	ZA12		
125	ZA13		
126	ZA14		
127	ZA15		
128	$\overline{SRES}$	I	
129	SEL1		
130	CLK	I/O	68000 interface signals.
131	SBCR	O	VIDEO+PSG
132	ZCLK	I/O	Z80 interface signals.
133	VSS	–	GND
134	MCLK	I	
135	EDCLK	I/O	
136	VDD	–	Power supply.
137	VD0	I/O	68000 data bus.
138	VD1		
139	VD2		
140	VD3		
141	VD4		
142	VD5		
143	VD6		
144	VD7		
145	VD8		
146	VD9		
147	VD10		
148	VD11		
149	VD12		
150	VD13		
151	VD14		
152	VD15		
153	VSS	–	GND
154	VA1	I/O	68000 address bus.
155	VA2		
156	VA3		
157	VA4		
158	VA5		

Pin No.	Name	I/O	Function
159	VA6	I/O	68000 address bus.
160	VA7		
161	VA8		
162	VA9		
163	VA10		
164	VA11		
165	VA12		
166	VA13		
167	VA14		
168	VA15		
169	VA16		
170	VA17		
171	VA18		
172	VA19		
173	VA20		
174	VA21		
175	VA22		
176	VA23		
177	SOUND	–	VIDEO+PSG
178	PSG (ANALOG)	O	
179	SOUND AVSS	–	
180	VSS	–	GND
181	$\overline{INT}$	O	Z80 interface signals.
182	$\overline{BR}$	O	68000 interface signals.
183	$\overline{BGACK}$	I/O	
184	$\overline{BG}$	I	
185	$\overline{IPL1}$	O	
186	$\overline{IPL2}$	I	
187	$\overline{IORQ}$	O	Z80 interface signals.
188	$\overline{ZRD}$	I	
189	$\overline{ZWR}$	I/O	
190	$\overline{M1}$	I	
191	$\overline{AS}$	I/O	68000 interface signals.
192	$\overline{UDS}$		
193	$\overline{LDS}$		
194	R/W		
195	$\overline{DTAK}$		
196	$\overline{UWR}$	O	P-SRAM interface.
197	$\overline{LWR}$	I/O	
198	$\overline{CASO}$	I/O	
199	$\overline{RASO}$	O	P-SRAM interface.
200	ZD0	I/O	Z80 data bus.
201	ZD1		
202	ZD2		
203	ZD3		
204	ZD4		
205	ZD5		
206	ZD6		
207	ZD7		
208	VDD	–	Power supply.

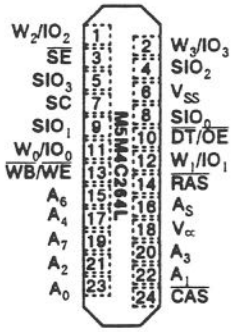
IC7/8 65536 Word × 4bit Dynamic RAM

IC M5M4C264L-12	IC M5M4C264L-15	IC UPD41264V-12	IC MB81461-12
IC HM53461ZP-12	IC TMS4461-12SDL	IC V53C261Z10	IC KM424C64Z-10
IC MSM51C262-10ZS	IC KM424C64Z-12		

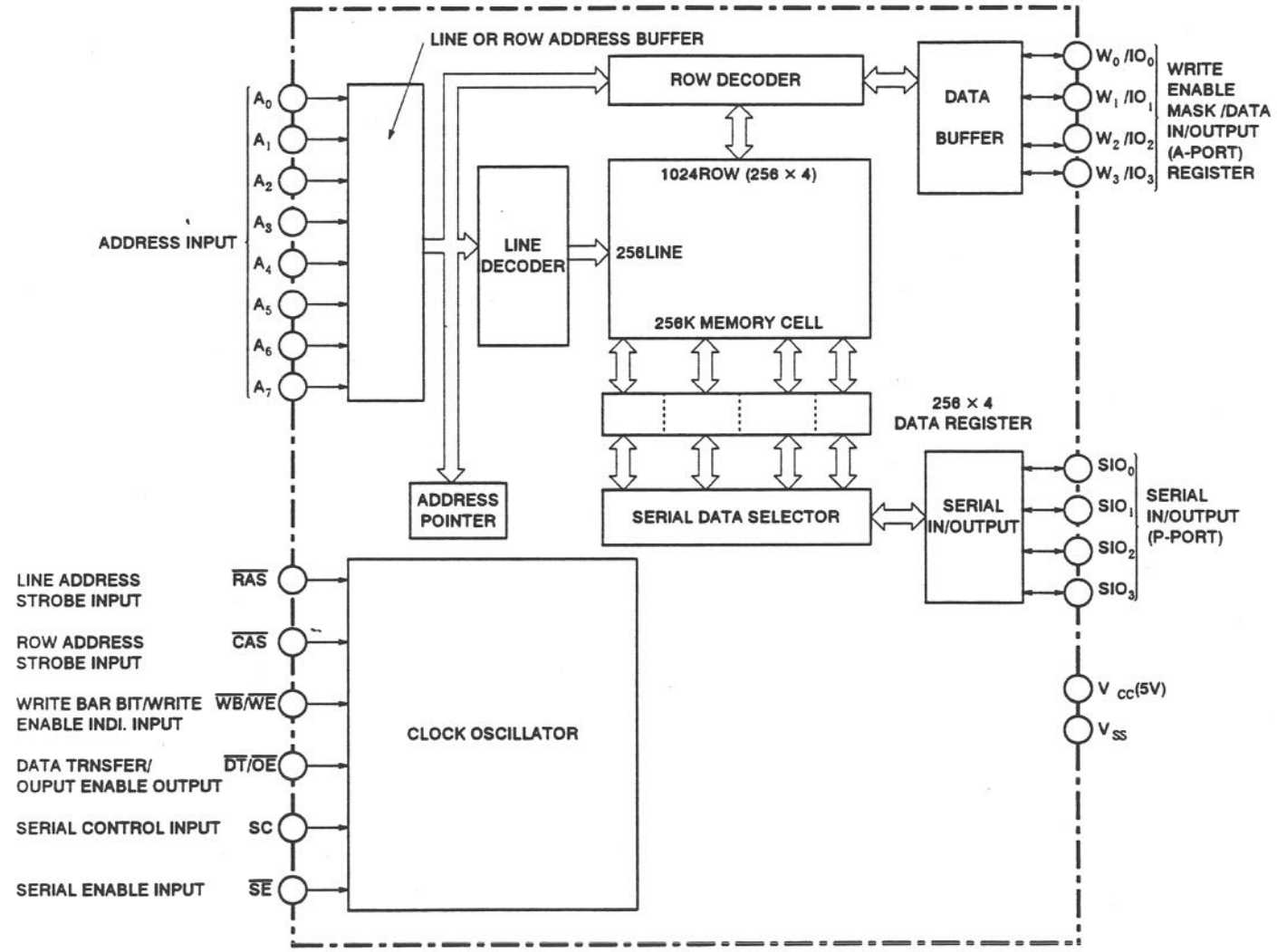
■ Outside View



■ Pin Layout



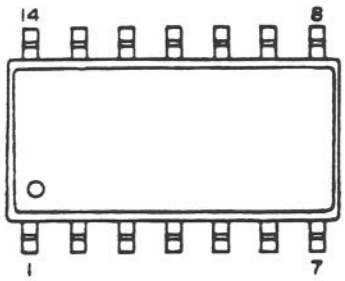
■ Block Diagram



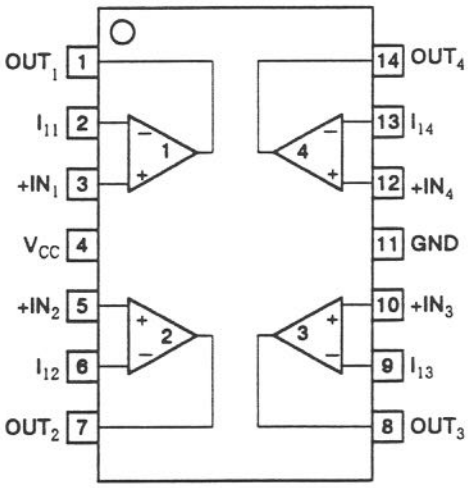
IC9/10 Quad Operational Amplifier

IC LM324

■ Top View



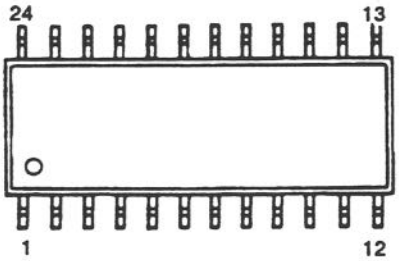
■ Pin Layout



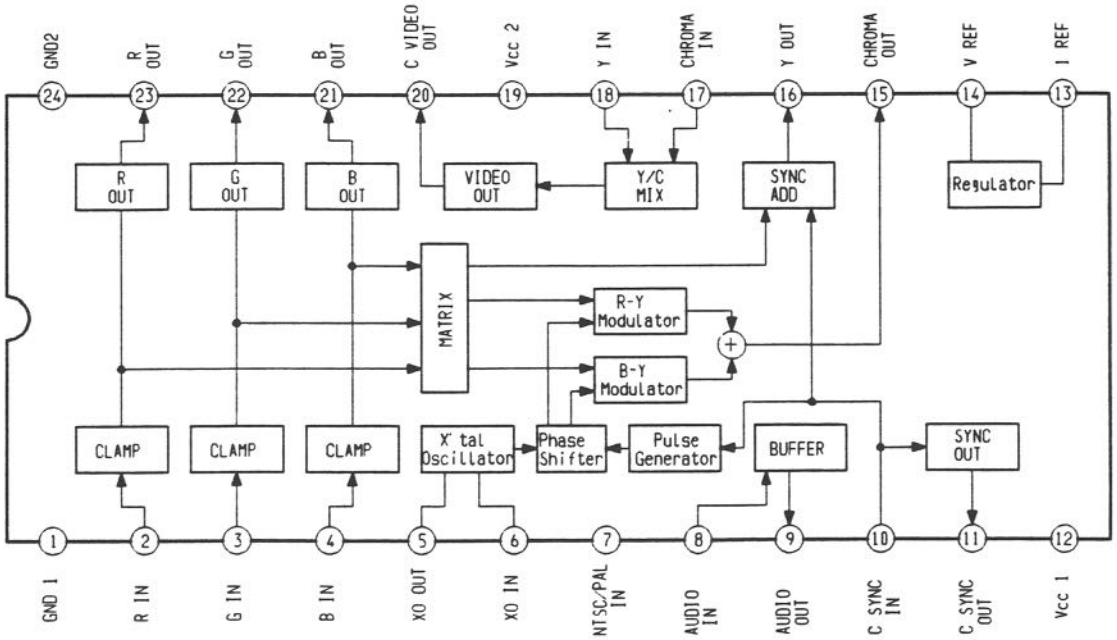
IC11 RGB Encoder

IC CXA1145M-T6

■ Top View



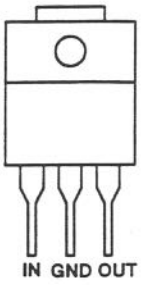
■ Pin Layout



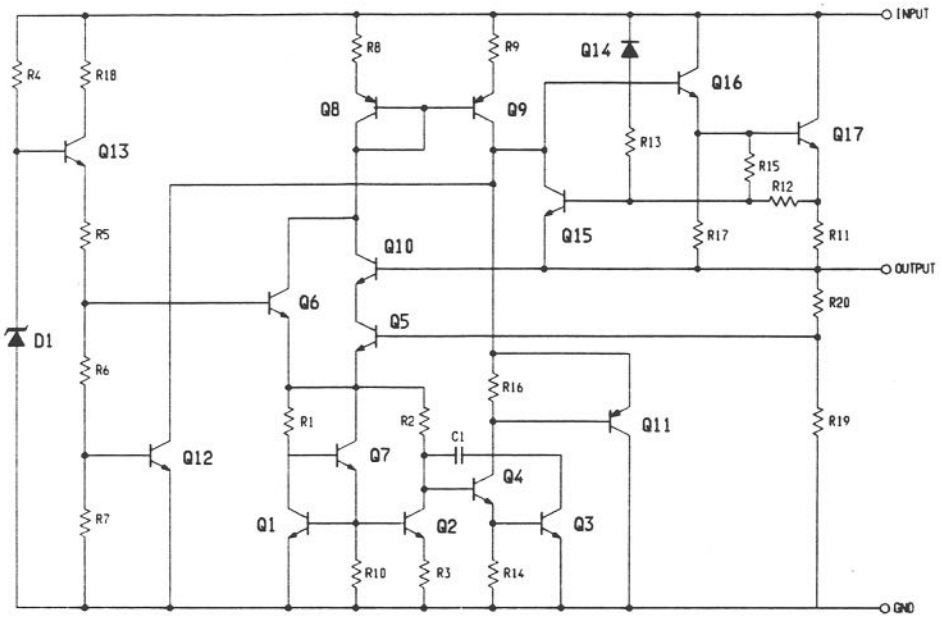
IC12

IC UPC7805HF

■ Top View



■ Block Diagram

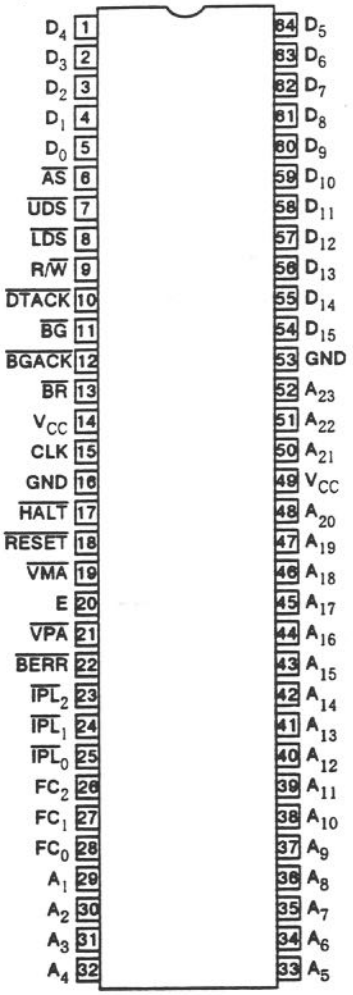


PARTS SPECIFICATIONS

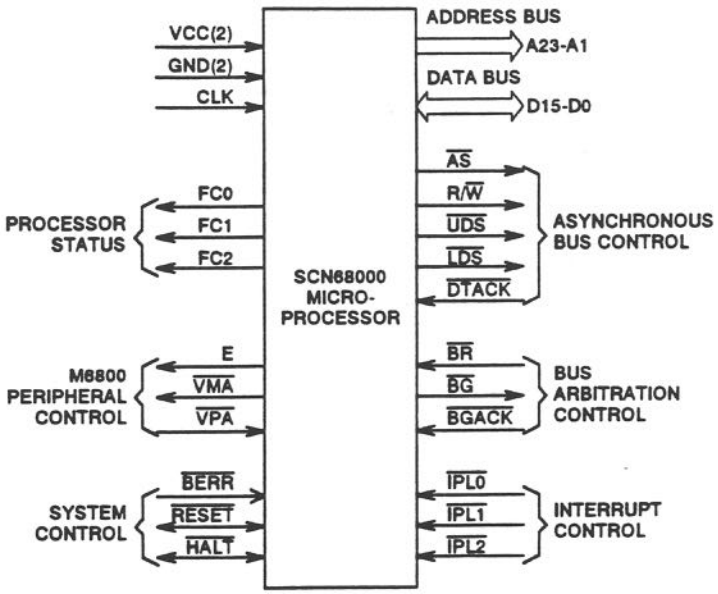
IC1 16/32-bit Microprocessor

IC SCN68000C8N64 IC MC68000P8

■ Top View & Pin Layout



■ Signal Description



■ Description

No.	Pin Name	I/O	Function
1	D_4	I/O	Data bus
2	D_3		
3	D_2		
4	D_1		
5	D_0		
6	$\overline{AS}$	O	Address strobe
7	$\overline{UDS}$	O	Upper data strobe
8	$\overline{LDS}$	O	Lower data strobe
9	$R/\overline{W}$	O	Read/write
10	$\overline{DTACK}$	I	Data transfer Acknowledge
11	$\overline{BG}$	O	Bus grant
12	$\overline{BGACK}$	I	Bus grant acknowledge
13	$\overline{BR}$	I	Bus request
14	V_{CC}	–	Power supply
15	CLK	I	Clock
16	V_{SS}	–	GND
17	$\overline{HALT}$	I/O	Halt
18	$\overline{RESET}$	I/O	Reset
19	$\overline{VMA}$	O	Vaild memory address
20	E	O	Enable
21	$\overline{VPA}$	I/OI	Vaild peripheral address

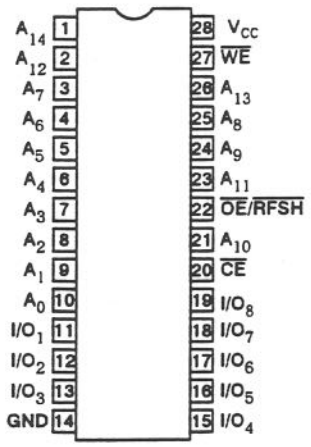
No.	Pin Name	I/O	Function
22	$\overline{BERR}$	I	Bus error
23	$\overline{IPL_2}$	I	Interrupt control
24	$\overline{IPL_1}$		
25	$\overline{IPL_0}$		
26	FC_2	O	Processor status
27	FC_1		
28	FC_0		
29	A_1	O	Address bus
30	A_2		
31	A_3		
32	A_4		
33	A_5		
34	A_6		
35	A_7		
36	A_8		
37	A_9		
38	A_{10}		
39	A_{11}		
40	A_{12}		
41	A_{13}		
42	A_{14}		
43	A_{15}		

No.	Pin Name	I/O	Function
44	A_{16}	O	Address bus
45	A_{17}		
46	A_{18}		
47	A_{19}		
48	A_{20}		
49	V_{CC}	–	Power supply
50	A_{21}	O	Address bus
51	A_{22}		
52	A_{23}		
53	V_{SS}	–	GND
54	D_{15}	I/O	Data bus
55	D_{14}		
56	D_{13}		
57	D_{12}		
58	D_{11}		
59	D_{10}		
60	D_9		
61	D_8		
62	D_7		
63	D_6		
64	D_5		

IC2/3 32768 Word × 8bit CMOS Pseudo-Static RAM

IC HM65256BSP-15 IC UPD42832C-15 IC TC51832-12

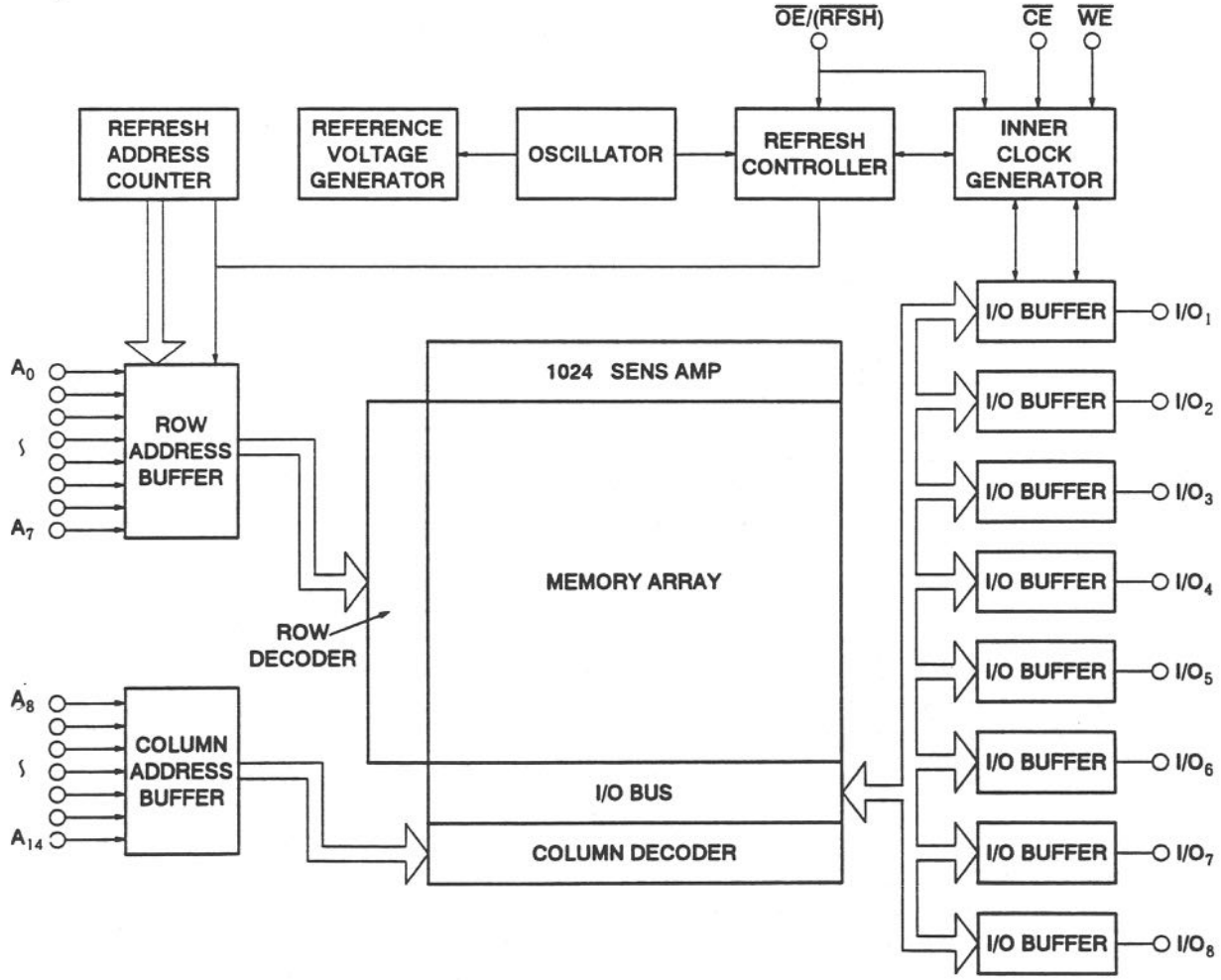
■ Top View & Pin Layout



■ Pin Name

Pin Name	Function
A0~A14	Address input
$\overline{WE}$	Write enable input
$\overline{OE}/\overline{RFSH}$	Output enable input/refresh input
$\overline{CE}$	Chip enable input
I/O1~I/O8	Data input/output
V_{CC}	Power supply
GND	Ground

■ Block Diagram

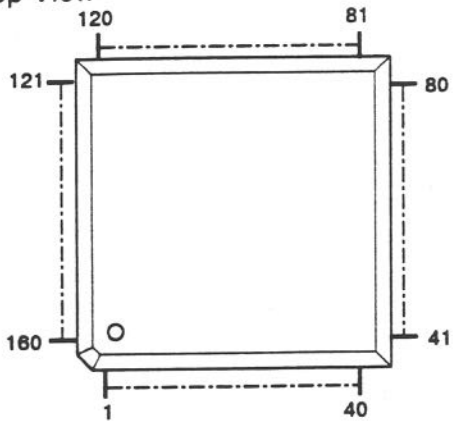


IC4

IC CUSTOM CHIP UPD92271

Parts No. : 315-5433

■ Top View



■ Pin Name

No.	Pin Name
1	VDD
2	MCLK
3	CART
4	ZRMM
5	XREF
6	XM1
7	ZRSS
8	XZBR
9	WAI
10	ZBAK
11	ZWW
12	ZRR
13	IREQ
14	MRQ
15	XNMI
16	ZD1
17	ZD0
18	ZD7
19	GND
20	VDD
21	GND
22	ZCLK
23	WRES
24	ZD2
25	ZD6
26	ZD5
27	ZD3
28	ZD4
29	ZAF
30	ZAE
31	ZAD
32	ZAC
33	ZAB
34	ZAA
35	ZA9
36	ZA8
37	ZA7
38	ZA6
39	ZA5
40	VDD

No.	Pin Name
41	GND
42	GND
43	ZA4
44	ZA3
45	ZA2
46	ZA1
47	ZA0
48	QA4
49	QA6
50	QA0
51	QA1
52	QA2
53	QA3
54	QA5
55	QB4
56	QB6
57	QB0
58	QB1
59	QB2
60	QB3
61	QB5
62	QC0
63	QC1
64	QC2
65	QC3
66	QC4
67	QC5
68	QC6
69	TST0
70	TST1
71	TST2
72	XJAP
73	A01
74	A02
75	A03
76	A04
77	A05
78	A06
79	GND
80	GND

No.	Pin Name
81	VDD
82	A07
83	A08
84	A09
85	A10
86	A11
87	A12
88	A13
89	A14
90	A15
91	A16
92	A17
93	A18
94	A19
95	A20
96	A21
97	A22
98	A23
99	GND
100	VDD
101	HL
102	XFDW
103	XFDC
104	XDIS
105	FRES
106	VDPM
107	XROM
108	ASEL
109	XTIM
110	RAS2
111	CAS2
112	XOE0
113	CAS0
114	SRES
115	XCE0
116	XLWR
117	IA14
118	XNOE
119	XEOE
120	VDD

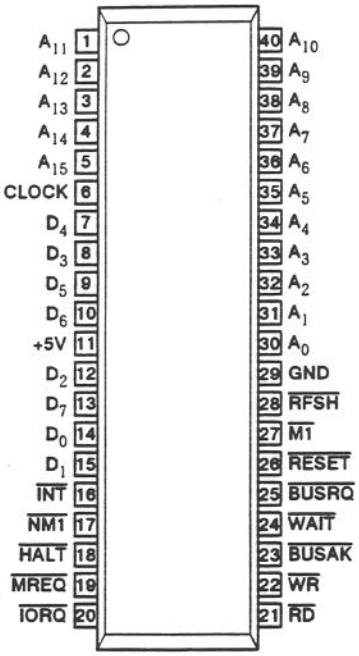
No.	Pin Name
121	GND
122	GND
123	VCLK
124	XM3
125	XAS
126	LDS
127	UDS
128	RW0
129	DTK
130	BG
131	BGA
132	BR
133	HALT
134	VRES
135	XVPA
136	FC0
137	FC1
138	D00
139	D01
140	D02
141	D03
142	D04
143	D05
144	D06
145	D07
146	D08
147	D09
148	D10
149	D11
150	D12
151	D13
152	D14
153	D15
154	NTS
155	HSYC
156	SOUN
157	INTA
158	EDCK
159	GND
160	GND

IC6 Z80A Central Processing Unit

IC Z80A

Parts No. : 315-0041

■ Top View & Pin Layout



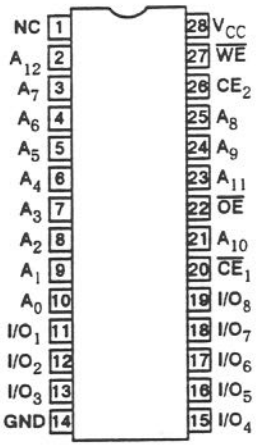
■ Description

Pin	Pin Name	I/O	Function
30~40 1~5	A0~A15	3-STATE O	System address bus.
15~12 7~10	D0-D7	3-STATE I/O	System data bus.
6	$\overline{\text{CLOCK}}$	I	Receives a +5V single-phase clock signal.
16	$\overline{\text{INT}}$	I	Active "Low". If the input/output device issues a signal that requests an interrupt to the Z80 CPU and the interrupt enable flag is zero, this interrupt request is accepted at the end of the instruction that is currently in progress.
17	$\overline{\text{NMI}}$	I	Active "Low". This is an interrupt request that has priority over $\overline{\text{INT}}$ and cannot be inhibited by the software. $\overline{\text{NMI}}$ is always accepted, and when the instruction that is currently in progress finishes, interrupt processing is started and the Z80 CPU automatically starts from address 0066H.
18	$\overline{\text{HALT}}$	O	Active "Low". This indicated that the HALT instruction is being executed. Executes the NOP instruction internally and also refreshes memory. The halt state is released by $\overline{\text{RESET}}$. $\overline{\text{NMI}}$ or $\overline{\text{INT}}$ (when enabled).
19	$\overline{\text{MREQ}}$	3-STATE O	Active "Low". This indicated that the address bus outputs the effective memory address for memory read/write.
20	$\overline{\text{IORQ}}$	3-STATE O	Active "Low". This indicates that the low-order 8 bits of the address bus output effective addresses of the input/output device for the read/write operation with this device. This is output together with $\overline{\text{MI}}$ during an interrupt response to indicate the response.
21	$\overline{\text{RD}}$	3-STATE O	Active "Low". This indicates the timing with which data from the memory or input/output device is read.
22	$\overline{\text{WR}}$	3-STATE O	Active "Low". This indicates that the effective data to be written to the memory or input/output device the address of which is specified is on the data bus.
23	$\overline{\text{BUSAK}}$	O	When the bus request is acknowledged, this informs the bus master which outputs the bus request that the system bus can be controlled.
24	$\overline{\text{WAIT}}$	I	Active "Low". Signal to inform the CPU that the memory or input/output device the address of which is specified is not ready to send data. The CPU is waiting when this signal is input.
25	$\overline{\text{BUSRQ}}$	I	Active "Low". This has priority over $\overline{\text{NMI}}$ and is accepted at the end of the machine cycle that is currently in progress. This is set to "Low" when a bus master other than the CPU wants to control the system bus.
26	$\overline{\text{RESET}}$	I	Active "Low". This resets the interrupt enable flag, interrupt vector register and memory refresh register of the program counter to set the interrupt mode to mode 0, thus initializing the Z80 CPU.
27	$\overline{\text{MI}}$	O	Active "Low". This indicates that the machine cycle being executed is an OP code fetch cycle.
28	$\overline{\text{RFSH}}$	O	Active "Low". This indicates that the address for refreshing the dynamic RAM is output to the low-order 7 bits of the address bus. $\overline{\text{MREQ}}$ also goes "Low" at this time.

IC7 65536 bit Static CMOS RAM

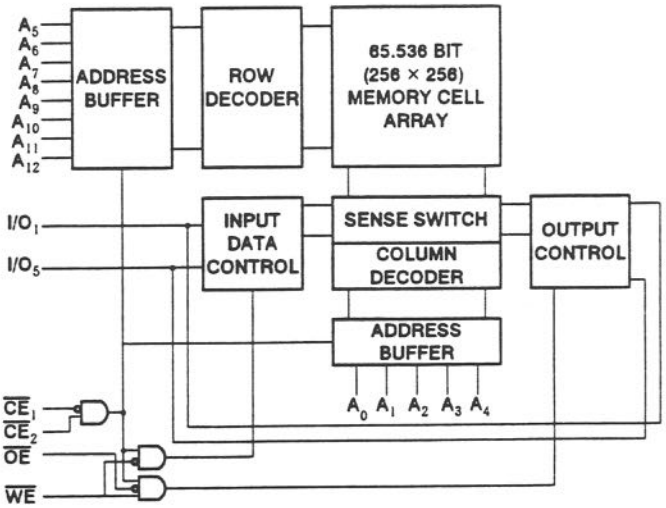
IC UPD4168C-20
IC UPD4364CX
IC HM6264L-120
IC HM6265L-90
IC UPD4168C-15
IC MB8464A-15L
IC KM6264BL-12 DIP600
IC HY6264LP-15
IC UPD4168C-15-SG
IC TMM2064-15
IC KM6264BLS-12L DIP300
IC KM4264L-15
IC UPD4364C-15
IC TMM2063-12

■ Top View & Pin Layout



A_0~A_{12}	: ADDRESS INPUT
OE	: OUTPUT ENABLE INPUT
I/O_1~I/O_8	: DATA IN/OUTPUT
V_{CC}	: +5V POWER SUPPLY
$\overline{CE}_1$, CE_2	: CHIP ENABLE 1, 2 INPUT
GND	: GROUND
$\overline{WE}$	: WRITE ENABLE INPUT
NC	: NO CONNECTION

■ Block Diagram



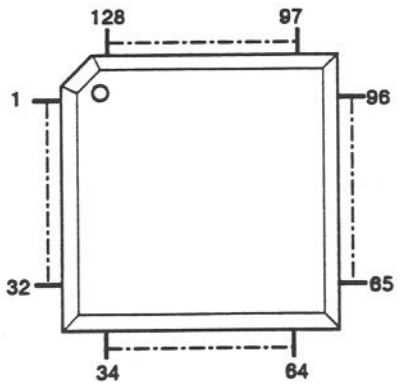
■ Operation Mode

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	MODE	OUTPUT STATE	POWER SUPPLY CURRENT
H	×	×	×	Non-select (Power down)	High impedance	I_{SB}
×	L	×	×			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

IC8 CUSTOM IC

IC CUSTOM CHIP YM7101
Parts No. : 315-5313

■ Top View & Pin Layout



■ Description

No.	Pin Name	I/O	Function
1	SD_0	I	VRAM serial data bus.
2	SD_1		
3	SD_2		
4	SD_3		
5	SD_4		
6	SD_5		
7	SD_6		
8	SD_8		
9	$\overline{SE_1}$	O	VRAM strobe/control.
10	$\overline{SE_0}$		
11	$\overline{SC}$		
12	$\overline{RAS_1}$		
13	$\overline{CAS_1}$		
14	$\overline{WE_1}$		
15	$\overline{WE_0}$		
16	$\overline{OE_1}$		
17	GND	–	GND
18	RD_0	I/O	VRAM data bus.
19	RD_1		
20	RD_2		
21	RD_3		
22	RD_4		
23	RD_5		
24	RD_6		
25	RD_7		
26	AGC	–	RGB analog GND.
27	R (ANLONG)	O	Linear RGB output.
28	G (ANLONG)		
29	B (ANLONG)		
30	AVC	–	RGB analog VDD.
31	AD_0	I/O	VRAM address/data bus.
32	AD_1		
33	AD_2		
34	AD_3		
35	AD_4		
36	AD_5		
37	AD_6		
38	AD_7		
39	$\overline{YS}$	O	Transparent output.
40	SPA/B	I/O	Sprite timing I/O.
41	$\overline{VSYNC}$	O	CRT Vsync out/dot clock out.
42	$\overline{CSYNC}$	I/O	VIDEO+PSG
43	$\overline{HSYNC}$	I/O	CRT HSYNC input/output
44	$\overline{HL}$	I	Light pen detect
45	SEL_0	I	CPU select (68000/Z80)
46	$\overline{PAL}$	I	CRT select (NTSC/PAL)
47	$\overline{RESET}$	I	Initial reset input.
48	SEL_1	I	68000 CPU clock (CLK1) I/O control.
49	CLK_1	I/O	68000 CPU clock (7.67MHz)

No.	Pin Name	I/O	Function
50	SBCR	O	Sub carrier output (4.47/3.58MHz clock)
51	CLK_0	O	Z80 CPU clock (3.58MHz)
52	MCK	I	Master clock input (53.7MHz).
53	EDCK	I/O	Dot clock input/output (13.4/10.7MHz).
54	VDD	I	Digital VDD.
55	CD_0	I/O	CPU data bus.
56	CD_1		
57	CD_2		
58	CD_3		
59	CD_4		
60	CD_5		
61	CD_6		
62	CD_7		
63	CD_8		
64	CD_9		
65	CD_{10}		
66	CD_{11}		
67	CD_{12}		
68	CD_{13}		
69	CD_{14}		
70	CD_{15}		
71	CA_0	I/O	CPU address bus.
72	CA_1		
73	CA_2		
74	CA_3		
75	CA_4		
76	CA_5		
77	CA_6		
78	CA_7		
79	CA_8		
80	CA_9		
81	CA_{10}		
82	CA_{11}		
83	CA_{12}		
84	CA_{13}		
85	CA_{14}		
86	CA_{15}		
87	CA_{16}		
88	CA_{17}		
89	CA_{18}		
90	CA_{19}		
91	CA_{20}		
92	CA_{21}		
93	CA_{22}		
94	AYS	I	Sound analog GND.
95	SOUND	O	Sound analog output.
96	AGS	I	Sound analog VDD.
97	GND	I	Digital GND.
98	$\overline{INT}$	O	Z80 interface.

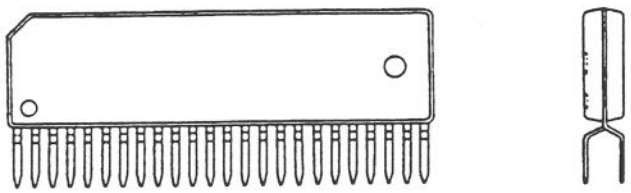
No.	Pin Name	I/O	Function
99	$\overline{BR}$	O	68000 interface.
100	$\overline{BGAK}$	I/O	
101	$\overline{BG}$	I	
102	$\overline{MREQ}$	I	Z80 interface.
103	$\overline{INTAK}$	I	68000 interface.
104	$\overline{IPL_1}$	O	
105	$\overline{IPL_2}$		
106	$\overline{IORQ}$	I	Z80 interface.
107	$\overline{RD}$		
108	$\overline{WR}$		
109	$\overline{M1}$		
110	$\overline{AS}$	I	68000 interface.
111	$\overline{UDS}$		
112	$\overline{LDS}$		
113	R/W		

No.	Pin Name	I/O	Function
114	$\overline{DTAK}$	I/O	68000 interface.
115	$\overline{UWR}$	O	Work RAM strobe control.
116	$\overline{LWR}$		
117	$\overline{OE0}$		
118	$\overline{CAS_0}$		
119	$\overline{RAS_0}$		
120	RA_0	O	Work RAM (DRAM) address/color code output.
121	RA_1		
122	RA_2		
123	RA_3		
124	RA_4		
125	RA_5		
126	RA_6		
127	RA_7		
128	VDD	I	Digital VDD.

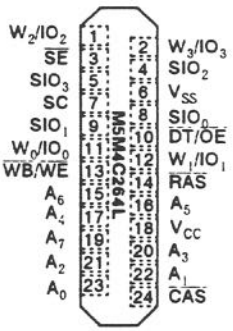
IC9/10 65536 Word × 4bit Dynamic RAM

IC M5M4C264L-12 IC M5M4C264L-15 IC UPD41264V-12 IC MB81461-12
IC HM53461ZP-12 IC TMS4461-12SDL IC V53C261Z10 IC KM424C64Z-10
IC MSM51C262-10ZS

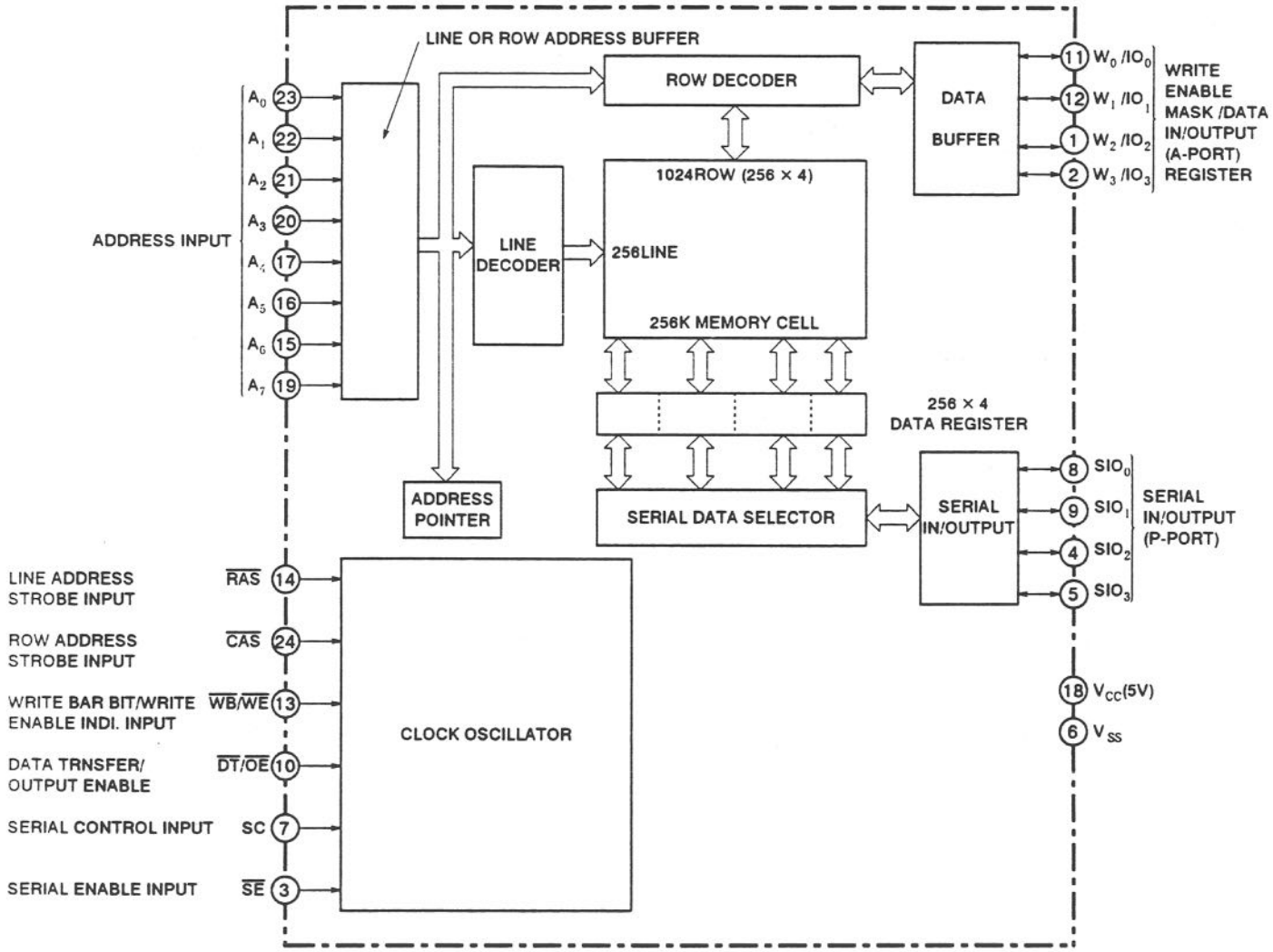
■ Outside View



■ Pin Layout



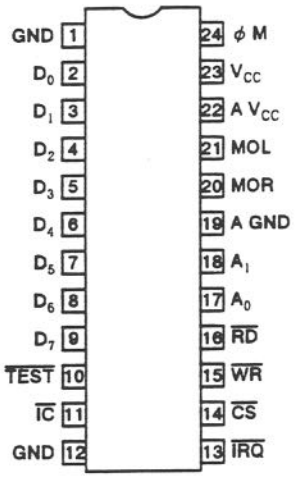
■ Block Diagram



IC11 FM Sound Source/DA Converter

IC YM2612

■ Top View & Pin Layout



■ Description

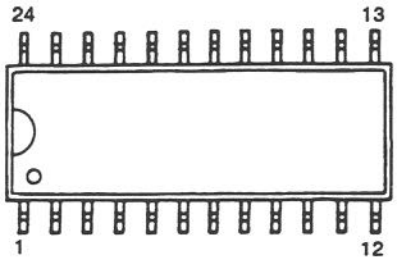
No.	Pin Name	I/O	Function
1	GND	–	Ground pin.
2	D_0	I/O	8-bit bidirectional data bus. Communicates data with the processor.
3	D_1		
4	D_2		
5	D_3		
6	D_4		
7	D_5		
8	D_6		
9	D_7		
10	$\overline{TEST}$	I/O	Pin to test this LSI. Do not connect.
11	$\overline{IC}$	I	Initializes the internal register.
12	GND	–	Ground pin.
13	$\overline{IRQ}$	O	Interrupt signal issued from the two timers. When the time programmed into the timer has elapsed, this goes low. Output with open drain.
14	$\overline{CS}$	I	Control the D0 – D7 data bus.
15	$\overline{WR}$		
16	$\overline{RD}$		
17	A_0		
18	A_1		
19	A GND	–	Ground pin.
20	MOR	O	Two-channel analog outputs. These are output with a source follower.
21	MOL		
22	A V_{CC}	–	+5V power supply pins.
23			
24	φ M V_{CC}	I	Master clock input.

CS	RD	WR	A1	A0	Details
0	1	0	0	0	Writes register addresses of timers, etc.
					Writes register addresses of channels 1-3.
0	1	0	0	1	Writes register data of timers, etc.
					Writes register data of channels 1-3.
0	1	0	1	0	Writes register addresses of channels 4-6.
0	1	0	1	1	Writes register data of channels 4-6.
0	0	1	0	0	Reads statuses.
1	X	X	X	X	D0 – D7 are set to high-impedance.

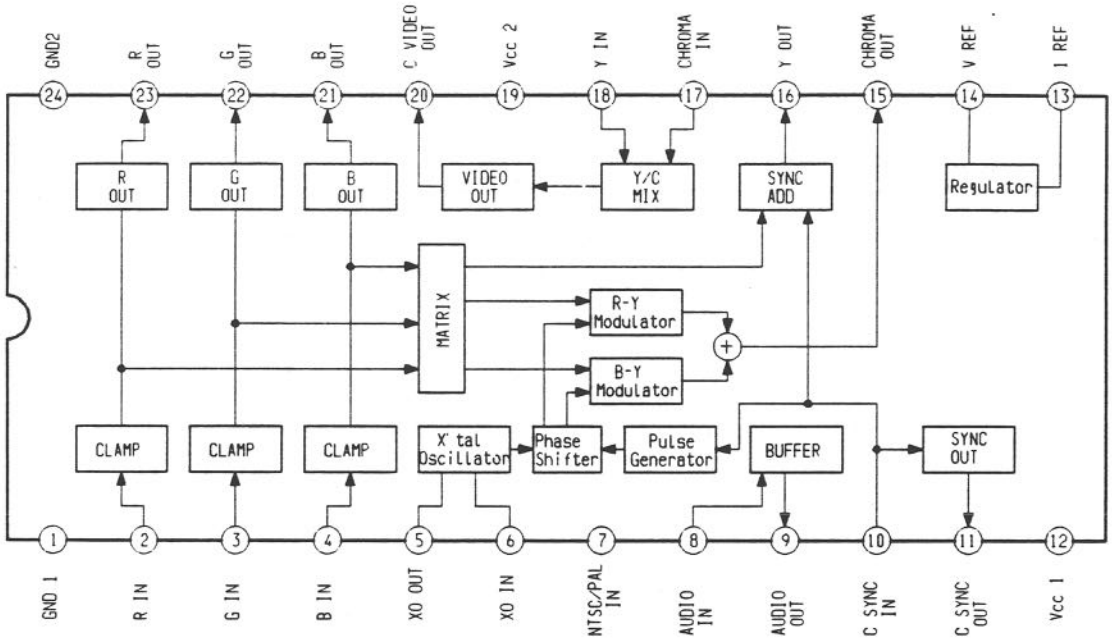
IC13 RGB Encoder

IC CXA1145P

■ Top View



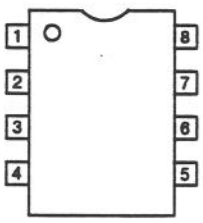
■ Pin Layout



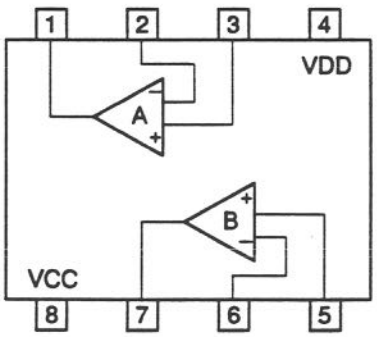
IC14 Dual Operational Amplifier

IC LM358

■ Top View



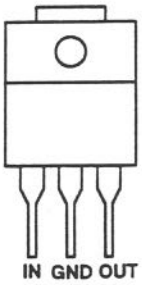
■ Pin Layout



IC15,17 Three Terminal Regulator

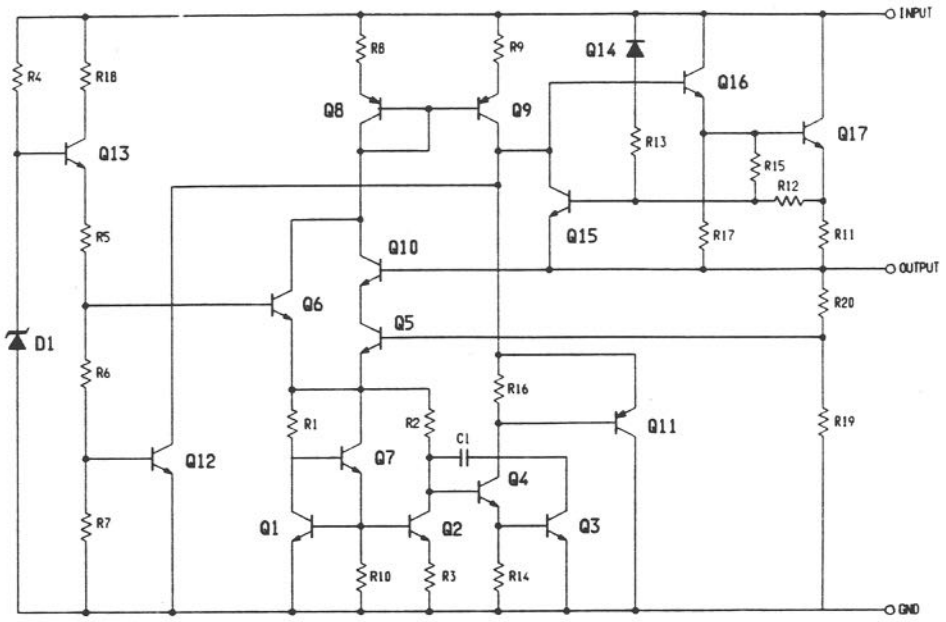
IC MA7805UC

■ Top View



IC MC7805CT

■ Block Diagram

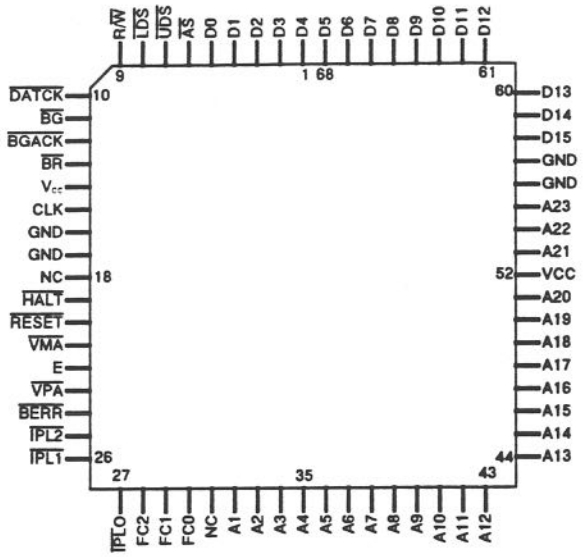


PARTS SPECIFICATION

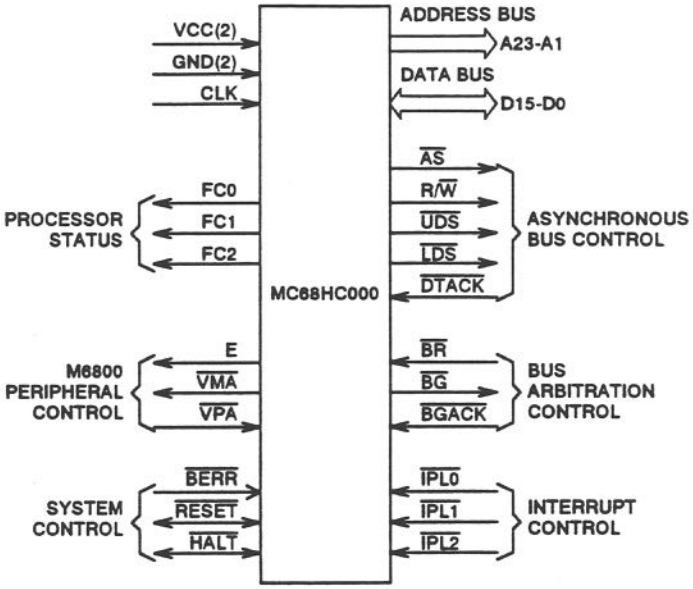
IC1 16/32-Bit Microprocessor

IC MC68HC000FN12 IC HD68HC000CP-12 IC TMP68HC000T-12

■ Top View & Pin Layout



■ Signal Description



■ Description

No.	Pin Name	I/O	Function
1	D_4	I/O	Data Bus
2	D_3		
3	D_2		
4	D_1		
5	D_0		
6	$\overline{AS}$	O	Address Strobe
7	$\overline{UDS}$	O	Upper Data Strobe
8	$\overline{LDS}$	O	Lower Data Strobe
9	R/$\overline{W}$	O	Read/Write
10	$\overline{DTACK}$	I	Data Transfer Acknowledge
11	$\overline{BG}$	O	Bus Grant
12	$\overline{BGACK}$	I	Bus Grant Acknowledge
13	$\overline{BR}$	I	Bus Request
14	V_{CC}	–	Power Supply
15	CLK	I	Clock
16	V_{SS}	–	GND
17	V_{SS}		
18	NC	–	Not Connected
19	$\overline{HALT}$	I/O	Halt
20	$\overline{RES}$	I/O	Reset
21	$\overline{VMA}$	O	Valid Memory Address
22	E	O	Enable

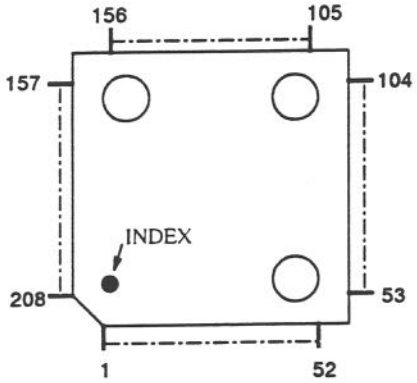
No.	Pin Name	I/O	Function
23	$\overline{VPA}$	I	Valid Peripheral Address
24	$\overline{BERR}$	I	Bus Error
25	$\overline{IPL_2}$	I	Interrupt Control
26	$\overline{IPL_1}$		
27	$\overline{IPL_0}$		
28	FC_2	O	Processor Status
29	FC_1		
30	FC_0		
31	N.C	–	
32	A_1	O	Address Bus
33	A_2		
34	A_3		
35	A_4		
36	A_5		
37	A_6		
38	A_7		
39	A_8		
40	A_9		
41	A_{10}		
42	A_{11}		
43	A_{12}		
44	A_{13}		
45	A_{14}		

No.	Pin Name	I/O	Function
46	A_{15}	O	Address Bus
47	A_{16}		
48	A_{17}		
49	A_{18}		
50	A_{19}		
51	A_{20}		
52	V_{CC}	–	Power Supply
53	A_{21}	O	Address Bus
54	A_{22}		
55	A_{23}		
56	V_{SS}	–	GND
57	V_{SS}		
58	D_{15}	I/O	Data Bus
59	D_{14}		
60	D_{13}		
61	D_{12}		
62	D_{11}		
63	D_{10}		
64	D_9		
65	D_8		
66	D_7		
67	D_6		
68	D_5		

IC2 CUSTOM CHIP MCE2

Parts No. : 315-5548

■ Top View



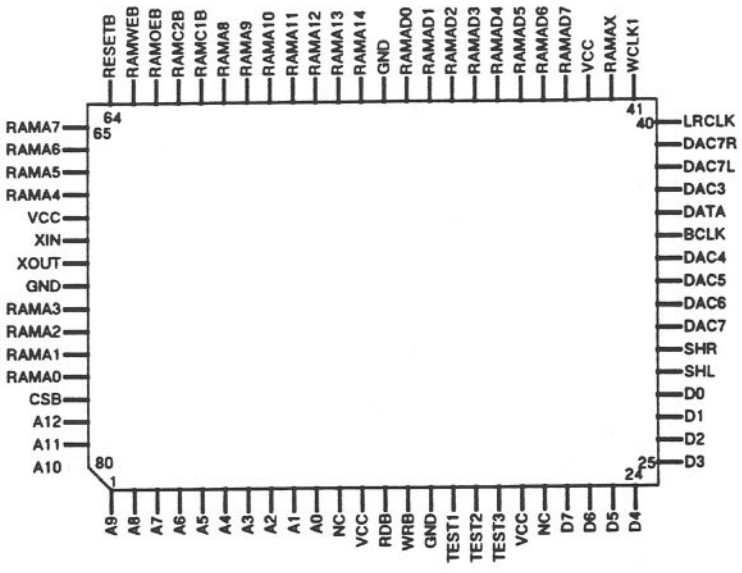
■ Description

No.	I/O	Pin Name
1	O	OCK25
2	O	OBRAM
3	–	V_{SS}
4	I	OXBROM
5	I	IROM
6	I	ICASO
7	I	ILWR
8	I	IUWR
9	I	IASEL
10	–	V_{DD}
11	I	IRAS2
12	I	ICAS2
13	I	IFDC
14	I	IFRES
15	–	V_{SS}
16	O	OERES
17	I/O	BEAD0
18	I/O	BEAD1
19	I/O	BEAD2
20	I/O	BEAD3
21	I/O	BEAD4
22	I/O	BEAD5
23	I/O	BEAD6
24	I/O	BEAD7
25	I/O	BED8
26	–	V_{SS}
27	–	V_{DD}
28	I/O	BED9
29	I/O	BED10
30	I/O	BED11
31	I/O	BED12
32	I/O	BED13
33	I/O	BED14
34	I/O	BED15
35	O	OERAS
36	O	OECAS
37	O	OEOE
38	–	V_{SS}
39	O	OEWE
40	O	OORAS
41	O	OOCAS
42	O	OOOE
43	–	V_{DD}
44	O	OOWE
45	I/O	BOAD0
46	I/O	BOAD1
47	I/O	BOAD2
48	I/O	BOAD3
49	I/O	BOAD4
50	–	V_{SS}
51	I/O	BOAD5
52	I/O	BOAD6
53	I/O	BOAD7
54	I/O	BOD8
55	I/O	BOD9
56	I/O	BOD10
57	I/O	BOD11
58	I/O	BOD12
59	I/O	BOD13
60	–	V_{SS}
61	–	V_{DD}
62	I/O	BOD14
63	I/O	BOD15
64	O	OLEDR
65	O	OLEDG
66	O	OLATCH
67	O	OSHFT
68	O	OATT
69	O	ODTM
70	I	IWFCK
71	I	ISCOR
72	–	V_{SS}
73	I	ISBSO
74	O	OEXCK
75	I	ILRCK
76	I	IDATA
77	I	IC2PO
78	I/O	BDB3
79	–	V_{DD}
80	I/O	BDB2
81	I/O	BDB1
82	I/O	BDB0
83	O	OHOCK
84	I	ICK50
85	–	V_{SS}
86	I	IIRQ
87	I	IDXM
88	I	ICDCK
89	O	OXPCM
90	I	IDTEN
91	I	IWAIT
92	O	OHRD
93	I	IINT
94	O	OCDC
95	O	OPROE
96	–	V_{SS}
97	–	V_{DD}
98	O	OC2LR
99	I	IA19
100	I	IA18
101	I	IA17
102	I	IA16
103	I	IA15
104	I	IA14
105	I/O	BA13
106	I/O	BA12
107	–	V_{SS}
108	I/O	BA11
109	I/O	BA10
110	I/O	BA9
111	I/O	BA8
112	I/O	BA7
113	I/O	BA6
114	–	V_{DD}
115	I/O	BA5
116	I/O	BA4
117	I/O	BA3
118	I/O	BA2
119	–	V_{SS}
120	I/O	BA1
121	I	IFC0
122	I	IFC1
123	O	OIPL0
124	O	OIPL1
125	O	OIPL2
126	O	OVPA
127	O	ORESET
128	O	OHALT
129	O	OCLK
130	–	V_{SS}
131	–	V_{DD}
132	O	ODTACK
133	I	IRXW
134	I	IXLDS
135	I	IXUDS
136	I	IXAS
137	I/O	BD0
138	I/O	BD1
139	I/O	BD2
140	I/O	BD3
141	I/O	BD4
142	–	V_{SS}
143	I/O	BD5
144	I/O	BD6
145	I/O	BD7
146	I/O	BD8
147	–	V_{DD}
148	I/O	BD9
149	I/O	BD10
150	I/O	BD11
151	I/O	BD12
152	I/O	BD13
153	I/O	BD14
154	–	V_{SS}
155	I/O	BD15
156	I/O	BPRA0
157	I/O	BPRA1
158	I/O	BPRA2
159	I/O	BPRA3
160	I/O	BPRA4
161	I/O	BPRA5
162	I/O	BPRA6
163	I/O	BPRA7
164	–	V_{SS}
165	–	V_{DD}
166	I/O	BPRA8
167	O	OPRRAS
168	O	OPRCAS
169	O	OPRUWE
170	O	OPRLWE
171	I/O	IVA1
172	I/O	IVA2
173	I/O	IVA3
174	I/O	IVA4
175	I/O	IVA5
176	–	V_{SS}
177	I/O	IVA6
178	I/O	IVA7
179	I/O	IVA8
180	I/O	IVA9
181	I/O	IVA10
182	I/O	IVA11
183	–	V_{DD}
184	I/O	IVA12
185	I/O	IVA13
186	I/O	IVA14
187	I/O	IVA15
188	I/O	IVA16
189	–	V_{SS}
190	I	IVA17
191	I/O	BVD0
192	I/O	BVD1
193	I/O	BVD2
194	I/O	BVD3
195	I/O	BVD4
196	I/O	BVD5
197	I/O	BVD6
198	I/O	BVD7
199	I/O	BVD8
200	–	V_{SS}
201	–	V_{DD}
202	I/O	BVD9
203	I/O	BVD10
204	I/O	BVD11
205	I/O	BVD12
206	I/O	BVD13
207	I/O	BVD14
208	I/O	BVD15

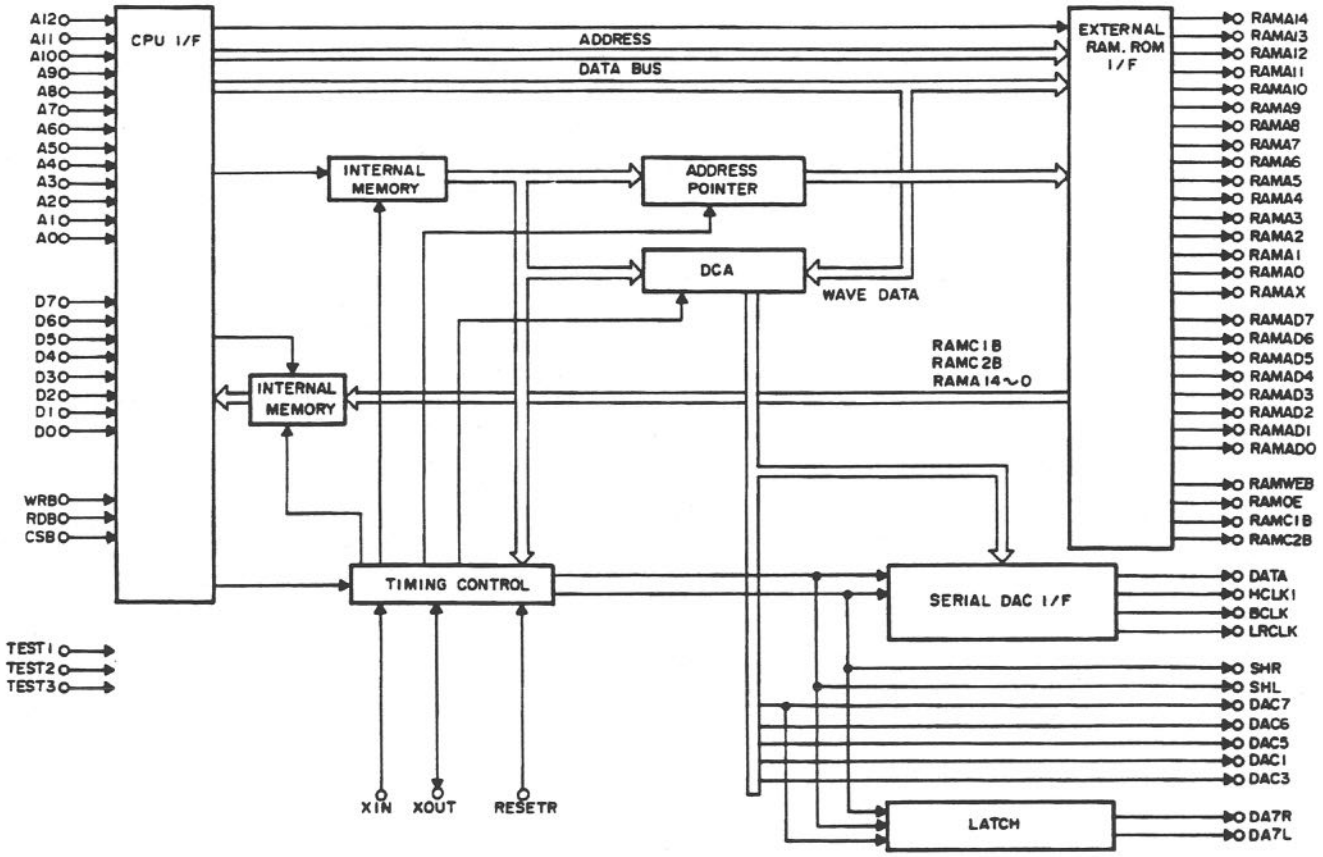
IC3 PCM Sound Source

IC RF5C164A
Parts No. : 315-5476A

■ Top View & Pin Layout



■ Block Diagram



■ Description (IC3)

Pin No.	Name	I/O	Function
78	A12	I	Address signals from μP.
79	A11		
80	A10		
1	A9		
2	A8		
3	A7		
4	A6		
5	A5		
6	A4		
7	A3		
8	A2		
9	A1		
10	A0		
21	D7	I/O	Data bus signals with μP.
22	D6		
23	D5		
24	D4		
25	D3		
26	D2		
27	D1		
28	D0		
77	CSB	I	Chip select signal from μP.
13	RDB	I	Read signal from μP.
14	WRB	I	Write signal from μP.
44	RAMAD7	I/O	When connected to a pseudo SRAM, these pins provide multiplex signals of the low order address/data to the SRAM, and when connected to an MROM, these pins provide data input signal from the MROM. When connected to an SRAM, these pins also provide data bus signals to the SRAM.
45	RAMAD6		
46	RAMAD5		
47	RAMAD4		
48	RAMAD3		
49	RAMAD2		
50	RAMAD1		
51	RAMAD0		
53	RAMA14	O	High order address signals of the SRAM & MROM.
54	RAMA13		
55	RAMA12		
56	RAMA11		
57	RAMA10		
58	RAMA9		
59	RAMA8		
65	RAMA7	O	Low address signals of the SRAM & MROM.
66	RAMA6		
67	RAMA5		
68	RAMA4		
73	RAMA3		
74	RAMA2		

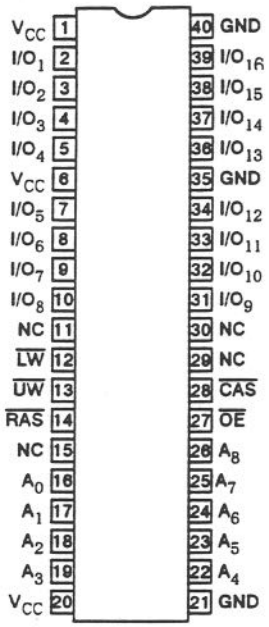
Pin No.	Name	I/O	Function
75	RAMA1	O	Low address signals of the SRAM & MROM.
76	RAMA0		
42	RAMAX	O	LSB address signal of the MROM.
61	RAMC2B	O	High order 32k byte SRAM & MROM select signal.
60	RAMC1B	O	Low order 32k byte SRAM & MROM select signal.
63	RAMWEB	O	Signal to write data to the pseudo SRAM or SRAM.
62	RAMOEB	O	Signal to read data from the pseudo SRAM, SRAM or MROM.
31	DAC7	O	Multiplex signals of "R" and "L" data output to the parallel DAC.
32	DAC6		
33	DAC5		
34	DAC4		
37	DAC3		
29	SHL	O	DAC7-3 "L" data sample/hold signal.
30	SHR	O	DAC7-3 "R" data sample/hold signal.
39	DAC7R	O	Signal obtained by sampling and holding the DAC7 output at SHR.
38	DAC7L	O	Signal obtained by sampling and holding the DAC7 output at SHL.
41	WCLK1	O	Word clock signal output to the serial DAC.
40	LRCLK	O	LR clock signal output to the serial DAC.
36	DATA	O	Digital audio data signal output to the serial DAC.
35	BCLK	O	Bit clock signal output to the serial DAC.
64	RESETB	I	Reset signal.
70	XIN	I	An external crystal oscillator is connected. A clock signal is input to XIN directly.
71	XOUT	O	
16	TEST1	I	Test signal inputs. Normally, fixed at "L". However, TEST2 is fixed at "H" when an MROM or SRAM is used.
17	TEST2		
18	TEST3		
12	VCC	–	Power supply pins.
19			
43			
69			
15	GND	–	Ground pins.
52			
72			

Note: The interface with the serial DAC is formed in the MSB initial mode.

IC5 CMOS Dynamic RAM

IC UPD424270LE-10

■ Top View & Pin Layout



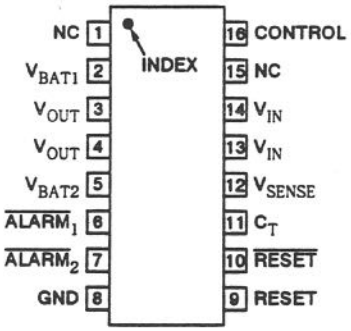
Input State				Output State	Operation Mode
$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$		
H	H	D	D	Open	Standby
H	L	H	H	Valid	Standby
L	L	H	H	Valid	Read cycle
L	L	L 2)	L 2)	Open	Early write cycle
L	L	L 2)	L 2)	Underlined	Delayed write cycle
L	L	H→L	H→L	Valid	Read modified write cycle
L	H	D	D	Open	$\overline{RAS}$ only refresh cycle
H→L	L	D	D	Open	$\overline{CAS}$ before /RAS refresh cycle
L	H→L	H	H	Valid	High-speed page mode read cycle
L	H→L	L 2)	L 2)	Open	High-speed page mode early write cycle
L	H→L	L 2)	L 2)	Underlined	High-speed page mode delayed write cycle
L	H→L	H→L	H→L	Valid	High-speed page mode read modified write cycle

Note: H=High(inactive), L=Low(active), D=Don't care.

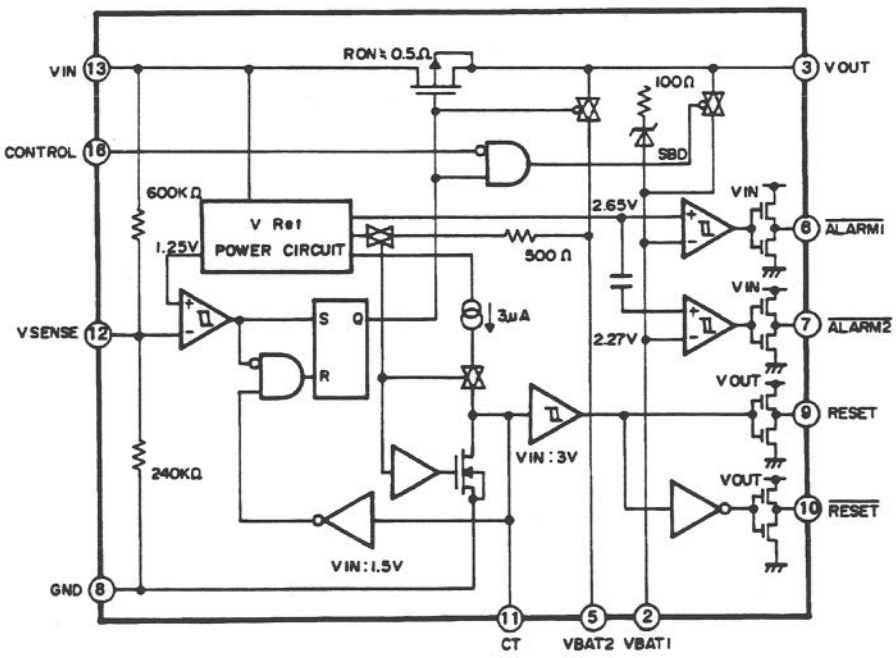
IC6 Battery Back-up

IC MB3790

■ Top View & Pin Layout



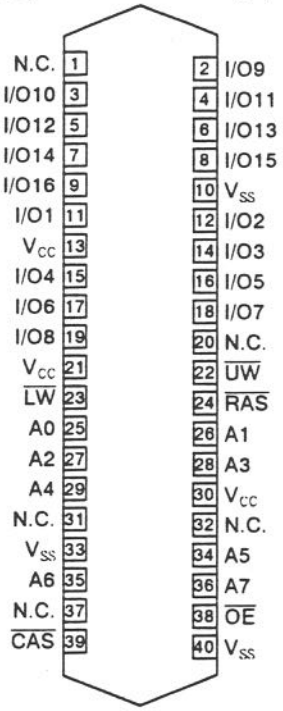
■ Block Diagram



IC 7/8 65536 Word × 16bit Dynamic RAM

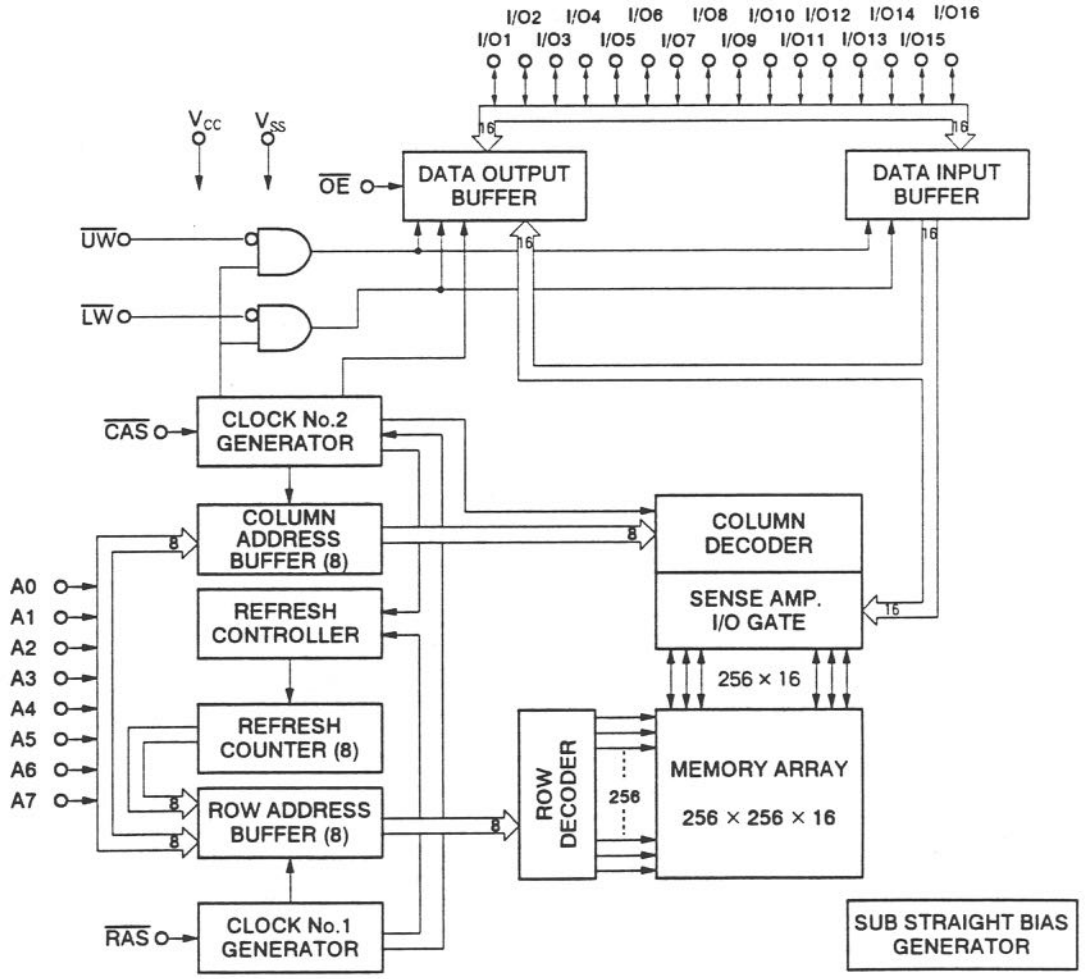
IC TC511664BZ-80 IC TC511664Z80

■ Top View & Pin Layout



■ Pin Name

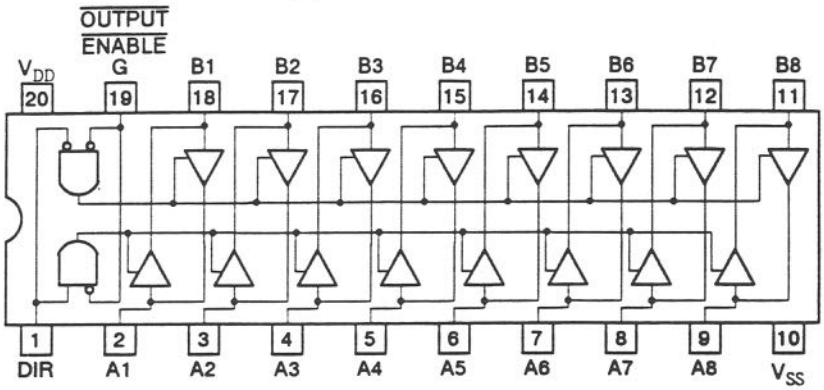
A0~A7	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Bit Write Input
$\overline{LW}$	Read/Lower Bit Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data I/O
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
N.C.	Not Connected



IC9 8-Circuits Non-Inverting Bus Tranceiver

IC 74HC245

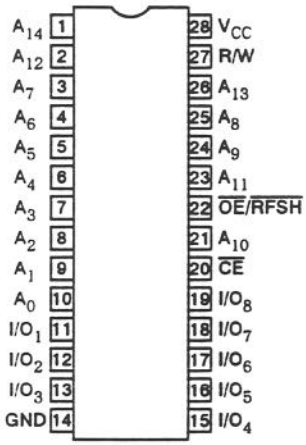
■ Top View & Pin Layout



IC10/11 8bit CMOS Pseudo Static RAM

IC TC51832AFL-10 IC TC51832FL-10

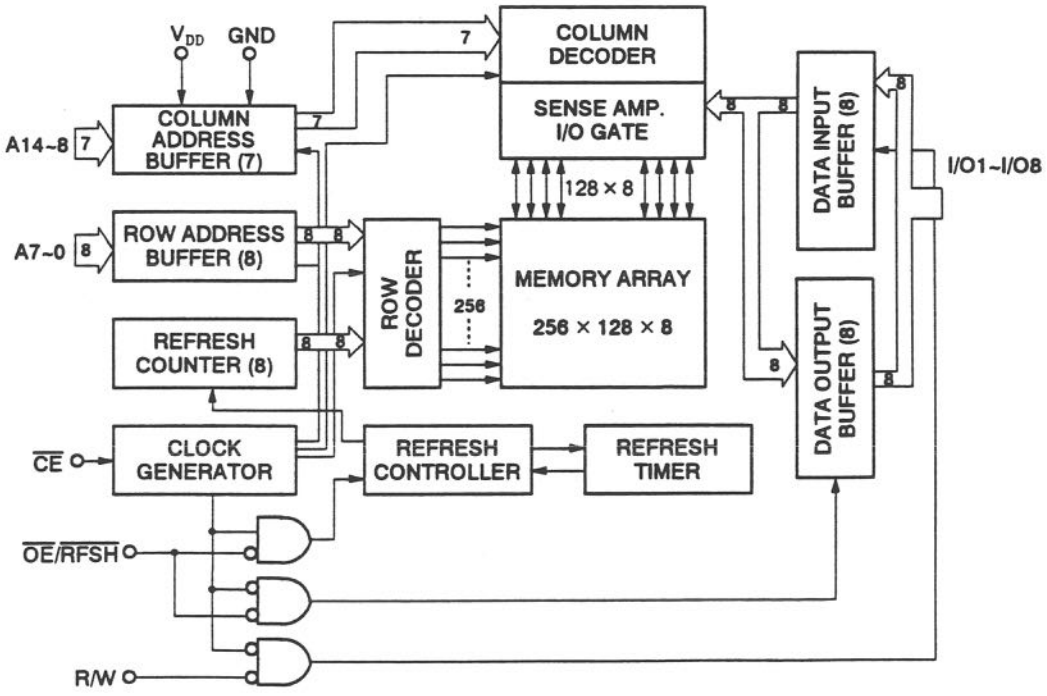
■ Top View & Pin Layout



■ Pin Configuration and Pin Description

Symbol	Pin Name
A_0~A_{14}	Address Input
R/W	Read / Write Input
$\overline{OE}$ / $\overline{RFSH}$	Output Enable / Refresh
$\overline{CE}$	Chip Enable
I/O_1~I/O_8	Data Input / Output

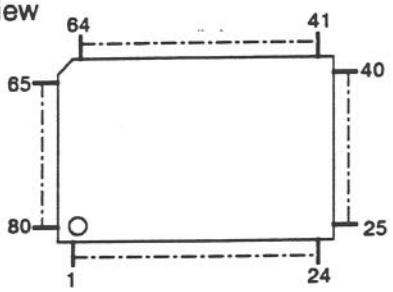
■ Block Diagram



IC13 CD-ROM LSI

IC LC8951

■ Top View



■ Description

No.	I/O	Pin Name
1	–	V_{SS}
2	O	RA6
3	O	RA7
4	O	RA8
5	O	RA9
6	O	RA10
7	O	RA11
8	O	RA12
9	O	RA13
10	O	RA14
11	O	RA15
12	O	$\overline{RWE}$
13	–	V_{SS}
14	O	$\overline{ROE}$
15	I/O	ERA
16	I/O	IO8
17	I/O	IO7
18	I/O	IO6
19	I/O	IO5
20	I/O	IO4

No.	I/O	Pin Name
21	I/O	IO3
22	I/O	IO2
23	I/O	IO1
24	–	V_{SS}
25	I	EXTAL
26	O	XTAL
27	I	TEST A
28	I	TEST B
29	I	CSEL
30	I	LMSEL
31	–	V_{DD}
32	I	LRCK
33	I	SDATA
34	I	BCK
35	I	C4LR
36	I	C2PO
37	O	MCK
38	I/O	D0
39	I/O	D1
40	I/O	D2

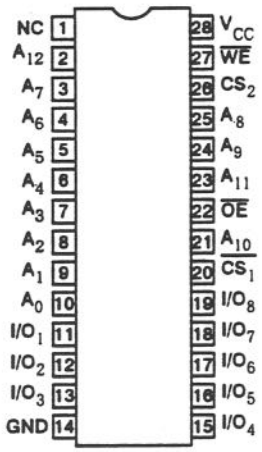
No.	I/O	Pin Name
41	–	V_{SS}
42	I/O	D3
43	I/O	D4
44	I/O	D5
45	I/O	D6
46	I/O	D7
47	I	RS
48	I	$\overline{RD}$
49	I	$\overline{WR}$
50	I	$\overline{CS}$
51	O	$\overline{INT}$
52	–	V_{SS}
53	I	$\overline{RESET}$
54	I	$\overline{ENABLE}$
55	I	$\overline{HRW}$
56	I	$\overline{HRD}$
57	I	$\overline{CMD}$
58	O	$\overline{WAIT}$
59	O	$\overline{DTEN}$
60	O	$\overline{STEN}$

No.	I/O	Pin Name
61	O	$\overline{EOP}$
62	O	$\overline{RCS}$
63	O	$\overline{HDE}$
64	–	V_{SS}
65	I/O	HD7
66	I/O	HD6
67	I/O	HD5
68	I/O	HD4
69	I/O	HD3
70	I/O	HD2
71	I/O	HD1
72	I/O	HD0
73	–	V_{DD}
74	I	$\overline{SELDRQ}$
75	O	RA0
76	O	RA1
77	O	RA2
78	O	RA3
79	O	RA4
80	O	RA5

IC14/15/16 64k(8k × 8)bit Static RAM

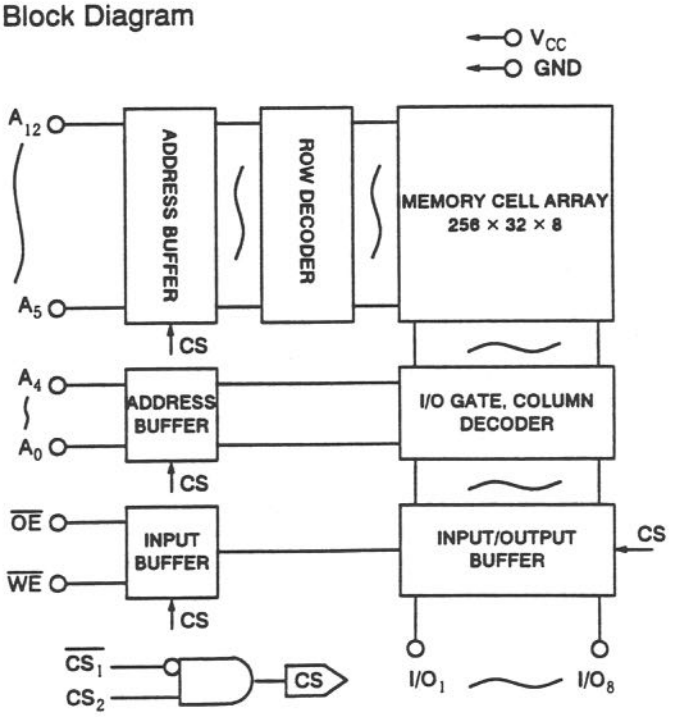
IC MB8464A-90 IC MB8464A-80 IC MB8464A-10LL PF-G-BND

■ Top View & Pin Layout



A_0-A_{12}	:Address inputs
I/O_1-I/O_8	:Data inputs/outputs
$\overline{CS_1}$	:Chip select 1
CS_2	:Chip select 2
$\overline{OE}$	:Output enable
$\overline{WE}$	:Write enable
V_{CC}	:Power supply (+5V)
GND	:Ground
NC	:Not connected

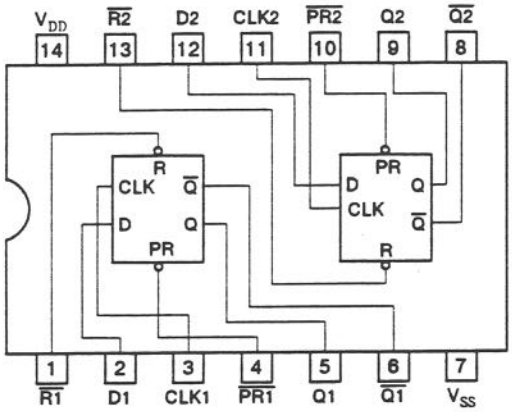
■ Block Diagram



IC17 2-Circuit D-type Flip-flop

IC 74AC74 IC74VHC74

■ Top View & Pin Layout



IC1/2 18Bit Digital Filter & 16Bit D/A Converter

IC LC7881M – C IC 7883KM

■ Top View

■ Description

Pin	Name	I/O	Function
1	CH1OUT	O	DAC CH-1 output.
2	VrefH	–	Reference voltage "H" input.
3	AVDD	–	Power supply of analog circuits.
4	DVDD	–	Power supply of digital circuits.
5	BLCK	I	Bit clock.
6	DATA	I	Digital audio data input. Input from the MSB in the bit serial state.
7	LRCK	I	L/R clock input. LRCK= "H" CH1 LRCK= "L" CH2
8	TEST	I	Test pin. (normally, set to "L")
9	ATT	I	Attenuator data input. Input from the LSB in the bit serial state.
10	SHIFT	I	Attenuator data transfer clock input.
11	LATCH	I	Attenuator data latch clock input.
12	INITB	I	Initializing signal input. (normally, set to "H")
13	TEST	I	Test pin. (normally, set to "L")

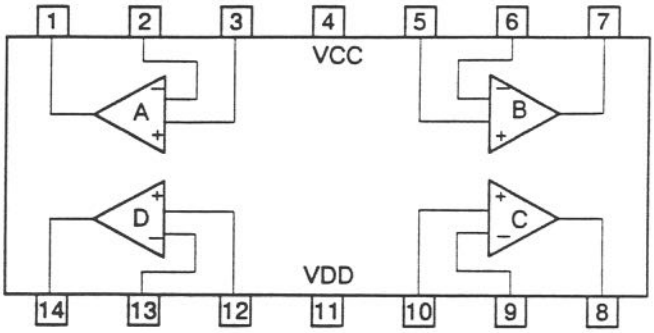
Pin	Name	I/O	Function
14	EMPH2	I	De-emphasis setting pins.
15	EMPH1		
16	D/N	I	Double/Normal speed switching pin.
17	SOC2	I	Input source select inputs. (PULL-DOWN)
18	SOC1		
19	MODE	I	Operation mode setting pin. (PULL-DOWN)
20	TEST	I	Test pins. (normally, set to "L") (PULL-DOWN)
21			
22	DGND	–	Ground of digital circuits.
23	CLKOUT	O	Clock output. 392Fs: 1/2 XOUT 384Fs, 448Fs, 512Fs : XOUT
24	XIN	I	Crystal oscillator input.
25	XOUT	O	Crystal oscillator output.
26	AGND	–	Ground of analog circuits.
27	VrefL	–	Reference voltage "L" input.
28	CH2OUT	O	DAC CH-2 output.

IC3/4/5 Quad Operational Amplifier

IC UPC844G2

■ Top View

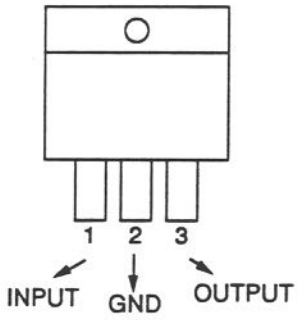
■ Pin Layout



IC6 3-Terminal Voltage Regulator

IC UPC2405HF

■ Front View



SEGA™

Printed in Japan (I)
40420